AMF

Venner

Digital Counter
Model 7737

MP MASTER
MA24445

DIGITAL COUNTER
MODEL 7737

Instruction Manual

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PREFACE

NOTE Notice of amendments applicable to this manual will be presented on pages marked 'CORRIGENDA' and bound immediately before the rear cover.

MODEL 7737 & VARIANTS K,L,Y & Z:

This instruction manual covers the standard DIGITAL COUNTER MODEL 7737 and variant forms that carry special features denoted by type number suffixes listed below.

K: Temperature compensated 10MHZ oscillator

L: Oven controlled 10MHz oscillator

Y: Data output - serial form

Z: Data output - parallel form

Model 7737A :

The manual also covers Model 7737A, which is identical to the standard instrument except that plug-in Counter card type 77/710 is fitted in place of Counter card type 77/700.

Counter type 77/710 is capable of higher frequency operation than the other counter. Consequently for Model 7737A , the maximum input frequency specified for functions FREQUENCY and COUNT is 80MHz; therefore, the following amendments are applicable to the SPECIFICATION commencing on page 2.

Section	Sub-heading	Amendment
2.3.1 and 2.3.4	Max. Frequency :	80MHz
2.4.1	Frequency range:	10Hz to 80MHz sinewave, D.C. to 80MHz pulse.

APPENDIX: COUNTER TYPE 77/710:

A description of Counter type 77/710 together with associated diagrams and components list are provided in the APPENDIX near the rear of this manual.

TABLE OF CONTENTS

Section		Page
1	INTRODUCTION	1
2	SPECIFICATION	2
	2.1 Power Supply	2
	2.2 Basic Functions	2
	2.3 Functional Characteristics	2
	2.3.1 Frequency	2
	2.3.2 Multi-period	2
	2.3.3 Timing	2
	2.3.4 Count	3
	2.4 Input Characteristics	3
	2.4.1 Input A	3
	2.4.2 Inputs B and C	4
	2.4.3 External Reference Input	4
	2.5 General Characteristics	4
	2.5.1 Display	4
	2.5.2 Display Time	4
	2.5.3 Display Storage	5
	2.5.4 Internal Reference Source	5
	2.5.5 Test Outputs	5
	2.5.6 Standard Frequency Output	5
	2.5.7 Data Output	6
	2.5.8 Temperature Range	6
	2.5.9 Size and Weight	6
3	OPERATION	7
	3.1 Mains-voltage Setting	7
	3.2 Mains-fuse Rating	8
	3.3 Connection and Switching of Mains Supply	8
	3.4 Warm-up Time	8
	3.5 Environmental Controls and Gate Lamp	8
	3.5.1 Frequency-standard Selector	8
	3.5.2 Slope Switch and Trigger Level Control	9
	3.5.3 Store Push-button	9
	3.5.4 Display Timer (and Display Dimming)	10
	3.5.5 Reset Push-button	10
	3.5.6 Gate Lamp	10
	3.6 Test Facility	11
	3.7 Measurements	12
	3.7.1 Frequency Measurement	12
	3.7.1.1 Principle of Operation	12
	3.7.1.2 Measurement Procedure	13
	3.7.2 Period/Multi-period Measurement	14
	3.7.2.1 Principle of Operation	14
	3.7.2.2 Measurement Procedure	14
	3.7.3 Timing	15
	3.7.3.1 Principle of Operation	15
	3.7.3.2 Measurement Procedure	16
	3.7.4 Count	17
	3.7.4.1 Principle of Operation	17
	3.7.4.2 Measurement Procedure	17

Section		Page
	3.8 Standard Frequency Output	18
	3.9 External Reference Facility	19
	3.10 Frequency Ratio Measurement	19
	3.11 Data Output Facility	21
4	MAINTENANCE	23
	4.1 Case Removal	23
	4.2 Fuse	23
	4.3 Plug-in Module Complement	23
	4.4 Preset D.C. Supplies - Adjustment	24
	4.5 Pulse Shaper Preset Control - Adjustment	25
	4.6 Oscillator Preset Control - Adjustment	26
	4.7 Preset Display Dimming Control - Adjustment	27
	4.8 Dismantlement	28
	4.8.1 Plug-in Cards	28
	4.8.2 Removal of Front Panel,Display Board & Pre-Amplifier	29
	4.8.3 Rear Panel Removal	29
	4.8.4 Power Unit Removal	30
5	CIRCUIT DESCRIPTION	31
	5.1 Circuit Diagrams and Nomenclature	31
	5.2 Supply Input Circuit	31
	5.3 Function Selection Circuit	32
	5.4 Pre-Amplifier Type 77/300	34
	5.5 Pulse Shaper Type 77/310	34
	5.6 Oscillator & Divider Types 77/500,510 and 511	36
	5.6.1 Oscillator & Divider Type 77/500	36
	5.6.2 Oscillator & Divider Types 77/510 and 77/511	38
	5.7 Divider Interface Type 77/400	38
	5.8 Stop & Start Shapers Type 77/320	40
	5.9 Gate Control & Reset Circuit Type 77/600	41
	5.10 Counter & Display Circuits Types 77/700,77/807 & 77/817	44
	5.11 Data Outputs	47
	5.11.1 Serial B.C.D. Interface Type 77/910	48
	5.11.2 Parallel B.C.D. Interface Type 77/900	48
	5.12 Circuit Logic Levels	49
6.	REPAIR	50
	6.1 Section Introduction	50
	6.2 Internal Supply Voltages	50
	6.3 Oscillator and Pulse Shaper Adjustment	50
	6.4 Control Line Voltages	50
	6.5 Plug-in Cards	52
	6.6 No-count condition and Malfunctions of the Display System	52
TABLES	Table 1: Test Function Displays	12
	Table 2: Control Line Voltages	51
APPENDIX:	Counter type 77/710 fitted in Model 7737A	

Section 7 ILLUSTRATIONS AND COMPONENTS LISTS

Title	Components List	Board(or card) Layout Dgm.	Drg.No.
Layout Diagram	-	-	S69/84
Rear Panel Assembly	CL 77/020	-	E68/93
Power Supply	CL 77/220	BL77/220	E68/92
Pre-Amplifier	CL 77/300	BL77/300	E68/95
Pulse Shaper	CL 77/310	BL77/310	E68/94
Oscillator & Divider:			
Type 77/500	CL 77/500	BL77/500	E69/02
Types 77/510 & 77/511	CL 77/510 & 77/511	BL77/510 &77/511	- E69/22
Divider Interface	CL 77/400	BL77/400	E68/100
Stop & Start Shapers	CL 77/320	BL77/320	E69/01
Gate Control & Reset	CL 77/600	BL77/600	E68/99
Counter & Scanning Display	-	-	E69/24
Counter	CL 77/700	BL77/700	E68/98
Display	CL 77/807	BL77/807	E68/96
Display Control	CL 77/817	BL77/817	E68/97
Serial BCD Interface	CL 77/910	BL77/910	E69/33
Parallel BCD Interface	CL 77/900	BL77/900	E69/27
Front Panel Assembly	CL 77/010	BL77/010*	E68/91
Function Control Diagram	-	-	E69/26
Signal Path Diagram	-	-	E69/25

* Switch Board of Front Panel Assembly

Section 1	INTRODUCTION

The Digital Counter Model 7737 carries comprehensive facilities for the measurement of frequency and frequency ratio, period (by single or multi-period sampling), timing and for general purpose counting.

Results are displayed by seven side-view neon indicator tubes: display storage is selectable.

The accuracy of all time dependent measurements is determined by the reference oscillator: the internal 10MHz crystal oscillator or an external frequency source. The instrument is supplied fitted with the standard oscillator, a temperature compensated oscillator (option K), or an oven-controlled oscillator (option L).

Slope selector and variable trigger level control with low-pass filter facility are provided at the main signal input.

The main functions of the instrument are selectable by means of push-buttons. A nine-position range selector and a display time control are provided. For the functions 'timing' and 'count' provision is made for the gating circuit to be operated by 'start' and 'stop' push-buttons or control signals applied to rear-mounted sockets at which slope selectors are provided.

A standard frequency output (selectable at the range switch in decade steps from 0.1Hz to 10MHz) is obtainable at a rear-mounted socket. Two test frequencies, obtainable at the front panel, enable the basic operations of the instrument to be checked.

Data output is an optional facility that is fitted only if it is initially ordered. Two types of output are available: serial output (option Y) and parallel output (option Z). The inclusion of an optional facility is denoted by the appendage of its code letter to the instrument type reference on the rear panel label.

Throughout the circuit of the instrument extensive use is made of integrated circuits: TTL for gating, and MOS-LSI for the general counting and frequency dividing functions.

Modular construction of the unit provides maximum accessibility of component parts for ease of servicing. A fold away tilt-stand is attached to the ventilated case, and the four instrument-rests provide for stowage of the supply cable.

Section 2	SPECIFICATION

2.1 POWER SUPPLY

100-125V/200-250V

45-60Hz/400Hz

Consumption: 20W

2.2 BASIC FUNCTIONS

Each function push-button selectable:

Frequency measurement

Multi-period measurement

Timing: (1) Single line

(2) Two-line

Count

2.3 FUNCTIONAL CHARACTERISTICS

2.3.1 Frequency

Input:	'A'
Max. Frequency:	50MHz
Gating time:	0.1µs to 10 sec. in decade steps
Accuracy:	$\pm$1 count $\pm$ crystal stability

2.3.2 Multi-period

Input:	'A'
Max. Frequency:	1MHz
Gating time:	1 to 10^7 periods in decade steps
Units of measurement:	0.1µs
Accuracy:	$\pm$0.1µs $\pm$ crystal stability

2.3.3 Timing

Time units:	0.1µs to 10 sec. in decade steps
Control inputs:	(1) Single-line: Input 'A'
	(2) Two-line: Start-input 'B' Stop-input 'C'
	or Push-buttons: 'Start' and 'Stop'
Accuracy:	$\pm$0.1µs $^{+0}_{-1}$ time unit
	$\pm$crystal stability

2.3.4 Count

Input:	'A'
Max. Frequency:	50MHz
Control Inputs:	Start-input 'B'
	Stop-input 'C' or
	Push-buttons: 'Start' and 'Stop'

2.4 INPUT CHARACTERISTICS

2.4.1 Input 'A'

Frequency range:	10Hz to 50MHz sinewave
	D.C. to 50MHz pulse
Input selection:	+ ; - ; ~
Sensitivity:	~: 10mV rms sinewave
	15mV peak pulse
	+ } 250mV rms sinewave
	- } 350mV peak pulse
Max. Input:	250V rms
Input Impedance:	1MΩ 30pF (approx.)
Input coupling:	A.C.
Max. d.c. level:	400V
Trigger slope:	Negative for '~' and ' - '
	Positive for ' + '
Trigger level:	~ Adjustable ±50mV (approx.)
	+ } Adjustable ±1V (approx.)
	- }
Frequency response:	Response limited at maximum positive trigger level. Sensitivity deteriorates above 10kHz at approx. 6dB/octave.
Paired pulse-resolution:	Typically better than 40ns (with pulse width 20ns and inter-pulse spacing 20ns).
Controls:	Trigger level/response: 3 position slope/sensitivity selector.

2.4.2 Inputs 'B' and 'C'

Frequency range:	100Hz to 5MHz (sinewave at rated sensitivity).
	D.C. to 5MHz pulse.
	Min. Pulse width 50ns.
Sensitivity:	500mV rms sinewave.
	1V peak pulse.
Max. Input:	100V peak
Min. Rate of rise:	0.5V/ms.
Input impedance:	20kΩ 60pF (approx.)
Input coupling:	A.C.
Max. d.c. level:	250V
Trigger slope:	Positive or negative
Controls:	Slope selection; Manual push-button.

2.4.3 External Reference Input

Frequency range:	100Hz to 10MHz (sinewave at rated sensitivity).
Sensitivity:	500mV rms sinewave.
	1V peak pulse
Max. Input:	100V peak.
Input impedance:	20kΩ, 60pF (approx.)
Input coupling:	A.C.
Max. d.c. level:	250V
Trigger slope:	Negative only.

2.5 GENERAL CHARACTERISTICS

2.5.1 Display

Seven digit display on sideview numerical indicator tubes. Integral decimal points automatically positioned by functional controls. Units of measurement indicated by switch settings. Gating indicator neon.

2.5.2 Display time

Adjustable 0.1 sec. to 5 sec. or infinite.

2.5.3 Display Storage

Switch-selected 'Normal' or 'Stored'

'Normal': Storage facility unused; display time as above.

'Stored': Readout retained until end of new sampling period.

2.5.4 Internal Reference Source

Internal reference (fitted as standard): 10MHz crystal controlled oscillator

Ageing rate: $\pm 1 \times 10^{-7}$ per month.

Temperature coefficient at $25^{\circ}C$ $\pm 3 \times 10^{-7}$ per $0^{\circ}C$ (typically).

Maximum drift ($-10^{\circ}C$ to $+55^{\circ}C$): $\pm 5 \times 10^{-6}$.

Option 'K': 10MHz temperature compensated oscillator.

Maximum drift ($0^{\circ}C$ to $+50^{\circ}C$): $\pm 1 \times 10^{-6}$.

Option 'L': 10MHz oven controlled oscillator.

Ageing rate: $\pm 1 \times 10^{-7}$ per month.

Stability: $\pm 1 \times 10^{-8}$ per $^{\circ}C$ max.

Maximum drift ($-10^{\circ}C$ to $+55^{\circ}C$): $\pm 3 \times 10^{-7}$.

2.5.5 Test Outputs

Frequency:

For Internal reference: (1) 10MHz (squarewave)

(2) 1MHz (squarewave)

For External reference: (1) Ext. ref. input frequency (squarewave)

(2) Ext. ref. input frequency $\div 10$ squarewave.

Amplitude (both outputs): 2.5V p-p min.

Output Impedance: Output 1 (10MHz): 500Ω

Output 2 (1MHz): 1kΩ

2.5.6 Standard Freq. Output

0.1Hz to 10MHz selectable in decade steps on FREQUENCY function (when using an internal oscillator or 10MHz external reference source). For output on other functions refer to Section 3.8.

Amplitude: 2.5V p-p min.

Waveform: Rectangular.

Output Impedance: TTL compatible (fan out of 10).

2.5.7 Data Output

Option 'Y':

Serial output.
4-wire b.c.d 1-2-4-8 code
('1' ≥ +3.5V; '0' ≤ +0.5V)*.
1-wire sequence start signal
(Positive 12V pulse),
1-wire clock signal(Negative 12V pulse),
1-wire print command(Negative 3.5V edge).

Option 'Z':

Parallel output.
4-wire per digit b.c.d. 1-2-4-8 code
('1' ≥ +2.5V; '0' ≤ +0.5V).
1-wire print command(Negative 3.5V edge).

2.5.8 Temperature Range

-10^{o} to $+55^{o}$ Centigrade.

2.5.9 Size and Weight

Width:	216mm.
Height:	89mm.
Depth:	289mm. (case) 310mm. (overall)
Weight:	4kg.

* Open-circuit d.c. levels with respect to chassis-earth

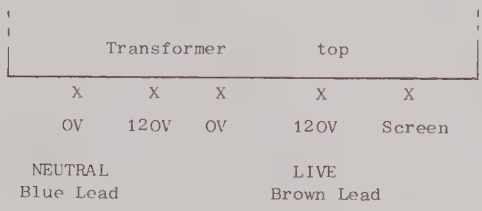
Section 3	OPERATION

3.1 MAINS-VOLTAGE SETTING

Before connecting a mains supply to the instrument check that the two primary windings of the internal transformer are appropriately connected for the supply voltage; proceed as follows.

Remove both sections of the instrument case, which is secured by screws at either side.

The transformer is mounted near the rear of the instrument. Terminations at the primary tags, which face the rear panel, are shown below (Note. Tags are represented by X's).



The primary windings should be linked in series or parallel according to the supply voltage. The appropriate links, which should be made by soldered wires, are as follows.

200-250V A.C. Supply:

Windings series connected. The 120V and 0V tags that lie between the LIVE and NEUTRAL tags should be linked together.

100-125V A.C. Supply:

Windings parallel connected. The two 0V tags should be linked together (NEUTRAL termination) and the two 120V tags should be linked together (LIVE termination).

The primary tags are accessible from the top of the instrument. If maximum access is required, remove the rear panel fixing screws (one in each corner of the panel) and unplug the entire rear panel assembly (complete with its surround) from the rear of the instrument.

When refitting the rear panel assembly, ensure that the rear-mounted power switch locates with its push-rod beside the transformer. Refit the instrument cover.

3.2 MAINS-FUSE RATING

Check that the mains fuse, mounted above the cable entry at the rear of the instrument, is suitable for the supply voltage; fuse ratings are as follows:

Supply Voltage		Fuse Rating
100-125V a.c.	:	600mA slow blow
200-250V a.c.	:	300mA " "

3.3 CONNECTION AND SWITCHING OF MAINS SUPPLY

The transformer connections (Section 3.1) and fuse rating (Section 3.2) having been checked, connect the three-core mains cable to the supply thus:

Brown core	:	LIVE
Blue core	:	NEUTRAL
Green and Yellow core	:	EARTH

A mains supply switch is contained within the instrument. To operate this switch, depress the push-button mounted below the legend POWER on the front panel. The indicator tubes should light up as the supply is switched on.

3.4 WARM-UP TIME

Measurements may be taken immediately after the supply has been switched on; however, for the accuracy of results to conform to the specification a period of at least fifteen minutes (for temperature stabilization of the internal reference oscillator circuit) should elapse before a measurement is taken.

No warm-up period is necessary for COUNT function or when an external standard frequency is used as reference source; in both circumstances the internal oscillator is unused.

3.5 ENVIRONMENTAL CONTROLS AND GATE LAMP

NOTE Controls not included in this section are treated in appropriate sub-sections under MEASUREMENTS.

3.5.1 Frequency-standard Selector

This rear-mounted switch (marked 'STD') enables either the internal oscillator (switch setting 'INT') or an external frequency source

(switch setting 'EXT') to be selected as frequency standard for all time dependent measurements.

For the 'EXT' setting signals from the external source should be applied to the coaxial socket below the 'STD' switch.

3.5.2 Slope Switch and Trigger Level Control

These two controls are applicable to signals received only at the A-Input socket.

The slope switch (three-position toggle switch) enables the operator to select the pulse-edge on which the instrument will be triggered: right-hand switch-position positive-going edge; centre position negative - going edge. The 'TRIGGER LEVEL' control may then be turned (from its centre position) in the direction corresponding to the selected pulse-edge until the instrument is triggered and a measurement is commenced: for example, when the slope switch is set to its centre position the TRIGGER LEVEL control should be turned anti-clockwise.

For the sinewave position of the slope switch (left hand position) triggering occurs on the negative-going edge of the waveform: the setting of the TRIGGER LEVEL control then determines where the trigger level will be: in the positive region, at the zero or transitional point, or in the negative region of the waveform.

Trigger Level LF Position

As the TRIGGER LEVEL control is turned fully-clockwise a ganged-switch is operated to bring into circuit a low pass filter. This setting, which corresponds to the adjacent panel-legend 'L.F.', is intended for low frequency inputs (up to approx. 10kHz) whose waveforms are subject to aberration (caused by h.f. content).

3.5.3 Store Push-button

NOTE This push-button (and each of the five push-buttons in the bank beside the 'TEST' sockets) will be automatically locked upon depression. It may be subsequently released by applying light momentary pressure.

When this push-button is in the released position (out) the indicator tubes display the progression and result of each count.

When the control is locked in the depressed position each count

is displayed until the end of the next gating period, whereupon the new count is shown. On this setting, no visible change will occur in the display if the new count is the same as the previous result.

If count-overflow occurs when the push-button is 'out' the indicator on the extreme left may be seen to reset from 9 to 0, but when the store facility is used no such evidence of overflow is available for only the final result, which is held by the internal counters, is made visible. It is, therefore, advisable to determine the magnitude of a measurement before making use of the store facility.

3.5.4 Display Timer (and Display Dimming)

The setting of this control determines the time for which each result is displayed. As the control is turned fully clockwise a ganged-switch is operated; on this setting, which corresponds to the panel legend 'INF' (Infinite), the display is retained until the 'RESET' push-button is operated.

NOTE A display dimming circuit is operated if more than one of the function push-buttons (FREQ., PERIOD, TIMING or COUNT) are depressed at any one time, or if the extreme anti-clockwise position of the range switch is used on 'PERIOD' function. Results shown by a dim display are invalid, for the condition indicates an incorrect setting of the controls.

3.5.5 Reset Push-button

Momentary depression of this push-button resets the instrument in readiness for a measurement. However, if the STORE push-button is in the depressed position when the RESET push-button is operated, the display circuit will not be affected: only the gating circuit and internal counters will be reset; the display will not change until a new measurement is shown at the end of the next gating period.

3.5.6 Gate Lamp

This neon lamp is illuminated for the duration of the gating period.

When the store facility is in use and consecutive measurements yield the same result, no change will occur in the display; however, the lamp

serves to indicate that gating action is occurring and, therefore, that the prolonged display may be accepted as the current result.

NOTE The lamp action will become less noticeable as very short gating times are selected.

3.6 TEST FACILITY

Two 'TEST' outputs '1MHz' and '10MHz' are available (at front-panel-mounted sockets) on all functions except 'TIMING'. Both outputs are derived from the reference frequency source: the '10MHz' directly, and the '1MHz' by way of a decade frequency divider.

The test outputs may be used to check the counting and readout operations of the instrument. To conduct the test proceed as follows.

(1) Establish the following control settings.

Control	:	Setting
'STD' switch	:	'INT'
Slope switch	:	Centre (negative-going)
'TRIG. LEVEL'	:	Mid-scale
'DISPLAY TIMER'	:	Mid-scale

(2) Connect the '10MHz' test output to the 'A-INPUT' socket (use coaxial cable).

(3) Depress the 'FREQ.' push-button (the control should lock in the depressed position). Take a measurement on each position of the range switch (nine-position rotary) and compare each result with the corresponding displays given under the appropriate heading in TABLE 1.

(4) Connect the 'A-INPUT' coaxial lead to the '1MHz' test socket. Repeat procedure (3) but for 'FREQ.' read 'PERIOD', and do not use the extreme anti-clockwise position of the range switch.

(5) Connect the 'A-INPUT' coaxial lead to the '10MHz' test socket. Set the rear-mounted 'START-B' and 'STOP-C' switches to '−'. Using coaxial cable feed the '1MHz' test output to both the 'START-B' and 'STOP-C' rear-mounted sockets. Repeat procedure (3) but for 'FREQ.' read 'COUNT'.
The result for COUNT should be: 0000010 ± 1.
This procedure may be repeated with the 'START-B' and 'STOP-C' switches set to '+'.

To check the operation of circuits actuated by the 'B' and 'C' push-buttons proceed as follows.

(1) Set the 'DISPLAY TIMER' to 'INF'

(2) Depress the 'TIMING B→C' push-button (the control should lock in the depressed position).

(3) Set the range switch to '1'.

(4) Momentarily depress the 'RESET' push-button.
Momentarily depress the 'START-B' push-button to initiate counting action. Observe the indicator on the extreme left; this should count repeatedly from 0 to 9, changing at the rate of one digit per second. Momentarily depress the 'STOP-C' push-button: counting should cease.

(5) Repeat procedure (4) for range switch settings 10 to 10^7, but the indicator that counts at the rate of one digit per second should be that situated one position further to the right for each new setting.

TABLE 1: Test Function Displays

RANGE SWITCH :	DISPLAYS	
SETTING	FREQ.	PERIOD
MHz x 10	0000001 ± 1	-
1	000001O ± 1	000001.0 ± 1
10	000010.0 ± 1	000010.0 ± 1
10^2	00010.00 ± 1	000100.0 ± 1
10^3	0010.000 ± 1	001000.0 ± 1
10^4	010000.0 ± 1	010000.0 ± 1
10^5	10000.00 ± 1	100000.0 ± 1
10^6	0000.000 ± 1	000000.0 ± 1
10^7	000000.0 ± 1	000000.0 ± 1

3.7 MEASUREMENTS

NOTE For warm-up time refer to Section 3.4.

3.7.1 Frequency Measurement

3.7.1.1 Principle of Operation

In this function the setting of the rotary range switch determines which of nine signal frequencies, derived from the standard frequency reference source, will control the internal gate; its setting therefore determines the gating time.

For the duration of the gating time, cycles of the 'A-INPUT' frequency pass through the gate to a chain of counter/indicator-drive circuits. The indicators display the resultant count; where appropriate a decimal point is included in the display so that the readout is shown in Hertz (Hz), kilo-Hertz (kHz) or mega-Hertz (MHz). Counts displayed on the highest range (MHz x 10) should be multiplied by ten for the result to be in mega-Hertz ; thus for example, the display 0000001 should be read as 10MHz.

3.7.1.2 Measurement Procedure

(1) Set the rear-mounted 'STD' switch to 'INT' if the internal oscillator is to function as reference source; if an external reference source is to be used, set the switch to 'EXT' and refer to Section 3.5.1.

(2) If a data logging output facility is to be used refer to Section 3.11.

(3) Set the 'DISPLAY TIMER' and 'STORE' push-button as required (for control functions refer to Sections 3.5.4 and 3.5.3).

(4) Apply the input signal to the coaxial 'A-INPUT' socket and set the adjacent slope switch to the required position (for control function refer to Section 3.5.2).

(5) Depress the 'FREQ' push-button.

(6) Set the range switch to a gating time for which the result will lie within the count capacity of the instrument(when the order of the input frequency is unknown the shortest gating time may be used first and the measurement then repeated on progressively lower ranges until the value is suitably resolved). The gating times for the range switch positions (in clockwise order) are listed below: the units of measurement for the various positions on frequency function are marked in black on the front panel.

Range Switch Position		Time
1	(MHz x 10)	0.1μs
2	(MHz)	1μs
3	"	10μs
4	"	100μs
5	"	1ms
6	(kHz)	10ms
7	"	100ms
8	"	1s
9	(Hz)	10s

(7) If the 'DISPLAY TIMER' is set to 'INF' momentarily depress the 'RESET' push-button.

(8) Adjust the setting of the 'TRIGGER LEVEL' control to suit the input waveform (for control use refer to Section 3.5.2). After a brief counting period the result of the measurement should be displayed.

3.7.2 Period/Multi-period Measurement

NOTE On 'PERIOD' function single period measurement is catered for by position '1' of the range switch (for which the count is recorded in 0.1μs units). Single period measurement may be taken also on function 'TIMING A→A' for which the time unit is selectable, refer to Section 3.7.3.2.

3.7.2.1 Principle of Operation

In this function signals applied to the 'A-INPUT', control the internal gate. The gate is held open for 'n' periods of the input waveform, where 'n' is the setting (for example 10^2) of the range switch. Throughout the gating time pulses derived from the standard frequency reference source, which occur at a rate of ten per microsecond, pass through the gate to a chain of counter/indicator drive circuits. The resultant readout is the time (in 0.1μs units) for which the gate was held open and is a period or multi-period measurement (according to the range switch setting) of the input waveform. A decimal point is included in the display so that the readout is in microsecond units.

3.7.2.2 Measurement Procedure

(1) Carry out procedures (1), (2), (3) and (4) of Section 3.7.1.2.

(2) Depress the 'PERIOD' push-button.

(3) Set the range switch to the number of periods (n) over which the measurement is to be taken; initially this number should be such that the result will lie within the count capacity of the instrument. (When the order of the input frequency is unknown a single period measurement may be taken initially, and the measurement then repeated over a progressively larger number of periods until the value is suitably resolved).

The values of 'n' are marked in blue around the range switch. The extreme anti-clockwise position of the switch is not for use on PERIOD function.

(4) If the 'DISPLAY TIMER' is set to 'INF' momentarily depress the 'RESET' push-button.

(5) Adjust the setting of the 'TRIGGER LEVEL' control to suit the input waveform (for control use refer to Section 3.5.2). After a brief counting period the result of the measurement should be displayed.

To obtain the time corresponding to a single period of the input waveform, the readout should be divided by the value of 'n' to which the range switch is set.

Measurement Example

Consider an input frequency in the order of 100kHz whose period is 10.2345678µs. If a measurement were taken first on the range n = 1 the resultant display would be 000010.2µs*. If the range $n = 10^6$ were then used, the count capacity would be exceeded ten times during the measurement and the resultant readout would be 234567.8µs*. Because this readout was obtained over 10^6 periods of the input waveform it should be divided by 10^6 to provide the value 0.2345678µs for one period. The first two digits determined on the first range (but occurring as overflow digits on the range 10^6) should then be appended to give 10.2345678µs as the period of the input signal.

3.7.3 Timing

3.7.3.1 Principle of Operation

Two modes of gating are available on 'TIMING' function.

On 'TIMING A→A' the gate is opened by the first pulse received at the 'A-INPUT' socket and closed by the second pulse.

On 'TIMING B→C' the gate is opened by a signal received at the 'B-INPUT' or by depression of the 'START' push-button: it is closed by a signal received at the 'C-INPUT' or by depression of the 'STOP' push-button.

Throughout the gating time, pulses derived from the standard frequency reference source pass through the gate (at a rate of ten pulses per microsecond) and through a frequency divider chain to counter/indicator-drive circuits. The range switch setting determines the effective division factor of the frequency divider chain and, therefore, the time unit of the count.

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* The display accuracy is specified in Section 2.3.2

Where appropriate a decimal point is included in the display so that the readout is in microseconds, milliseconds or seconds according to the setting of the range switch.

Results displayed on the highest range (s x 10) should be multiplied by ten for the measurement to be in seconds; thus, for example, the display 0000001 should be read as 10 seconds.

3.7.3.2 Measurement Procedure

(1) Carry out procedures (1), (2) and (3) of Section 3.7.1.2.

(2) Set the range switch for the required time unit.
For clockwise rotation of the range switch the time units are 0.1us to 10s in decade steps (as listed in Section 3.7.1.2 '6').

(3) Carry out the procedure given below under the timing mode to be used.

'TIMING A→A'

(a) Apply the input signal to the 'A-INPUT' socket and set the adjacent slope switch to the required position (for control function refer to Section 3.5.2)

(b) Depress the 'TIMING A→A' push-button.

(c) Adjust the setting of the 'TRIGGER LEVEL' control to suit the input waveform (for control use refer to Section 3.5.2).
If the 'DISPLAY TIMER' is set to 'INF' momentarily depress the 'RESET' push-button to enable the A-INPUT signals to initiate a measurement. For other settings of this control measurements should occur automatically.

'TIMING B→C'

Gating may be started and stopped manually by use of the appropriate push-buttons, or electronically by signals applied to the 'START-B' and 'STOP-C' sockets; alternatively the gate may be opened by one method and closed by the other. The sockets may be connected in parallel if single line gate control is required; then, the first of two successive signals on the line will open the gate and the second will close it. External leads to the 'START-B' and 'STOP-C' sockets should be as short as practicable and screened to minimise pick-up which otherwise might cause unwanted trigger

operation. It is recommended that, where practicable, external trigger circuits for these inputs be battery powered to eliminate the possibility of the instrument being triggered by spurious mains-initiated pulses or ripple.

NOTE The shaper circuits of the 'B' and 'C' inputs are designed to operate from low frequency sinusoidal signals down to 100Hz. To operate the instrument from square-wave signals of frequency less than 1kHz, it may be necessary to connect a capacitor (value range 800 pF to 1000 pF) in series with the 'B' and/or 'C' inputs so that the input signal will be differentiated.

(a) Connect a coaxial signal-cable to each rear-mounted socket ('START-B': 'STOP-C') that is to be used for gate control.

(b) Momentarily depress the 'RESET' push-button.

(c) Timing will commence when the 'B-START' push-button is momentarily depressed (or a signal is applied to the 'START-B' socket) and will cease when the 'C-STOP' push-button is momentarily depressed (or a signal is applied to the 'STOP-C' socket).

3.7.4 Count

3.7.4.1 Principle of Operation

On this function gating may be started and stopped manually by depression of the 'B-START' and 'C-STOP' push-buttons, or electronically by signals applied to the 'START-B' and 'STOP-C' sockets; alternatively the gate may be opened by one method and closed by the other.

Throughout the gating time signals received at the 'A-INPUT' socket pass through the gate to a chain of counter/indicator-drive circuits. The readout is therefore the number of 'A-INPUT' signals received during the gating time.

3.7.4.2 Measurement Procedure

(1) Carry out procedures (2),(3) and (4) of Section 3.7.1.2.

(2) Connect a coaxial signal cable to each rear-mounted socket ('START-B'; 'STOP-C') that is to be used for gate control. The 'Note' appearing under 'Timing B-C' in Section 3.7.3.2 is

applicable also to COUNT function.

(3) Depress the 'COUNT' push-button.

(4) Momentarily depress the 'RESET' push-button.

(5) Set the 'TRIGGER LEVEL' control to suit the input waveform (for control use refer to Section 3.5.2).

(6) To begin the gating period momentarily depress the 'B-START' push-button or apply a signal to the 'START-B' socket.

(7) To end the gating period momentarily depress the 'C-STOP' push-button or apply a signal to the 'STOP-C' socket.

3.8 STANDARD FREQUENCY OUTPUT

Standard frequency signals are available at the rear-mounted coaxial 'STD.FREQ.' socket on functions FREQUENCY and COUNT. The signals are also available on both TIMING functions but only throughout the period that the gate is held open. The signals are not available on PERIOD function.

The output signal frequency is dependent upon the setting of the range switch as indicated in the table below.

The source of the signals is determined by the setting of the 'STD' switch (refer to Section 3.5.1). Signals are derived from the reference source by decade frequency division; therefore, when an external reference standard is used its frequency should be 10MHz (otherwise the table below will not be valid).

NOTE The signals are momentarily interrupted whenever reset action occurs.

TABLE 2: Standard Frequency Output

Range Switch Positions (clockwise order)	Standard Frequency Output
1	10MHz
2	1 "
3	100kHz
4	10 "
5	1 "
6	100Hz
7	10 "
8	1 "
9	0.1 "

3.9 EXTERNAL REFERENCE FACILITY

When the rear-mounted switch marked 'STD' is set to 'INT' the internal 10MHz oscillator is employed as reference frequency source.

When the 'STD' switch is set to 'EXT' the internal oscillator is switched out of circuit and signals, from an external source, applied to the 'EXT' socket serve as reference signals for the instrument.

The external reference facility may be used to increase the accuracy of the instrument for the standard functions (by use of an external 10MHz source frequency the accuracy of which is superior to that of the internal oscillator; refer to Section 2.5.4) or to alter the significance of the readout so that the instrument may be operated in a non-standard manner (by use of an external source frequency other than 10MHz).

The facility may be used for frequency ratio measurement; the subject is treated in the following section.

3.10 FREQUENCY RATIO MEASUREMENT

To conduct a frequency ratio measurement for signals from two sources proceed as follows.

(1) Set the rear-mounted 'STD' switch to 'EXT'.

(2) Apply signals (f_S) from one source to the 'STD' socket.

(3) Apply signals (f_A) from the second source to the 'A INPUT' socket and set the adjacent slope switch to the required position (for control function refer to Section 3.5.2).

(4) If a data logging output facility is to be used refer to Section 3.11.

(5) Set the 'DISPLAY TIMER' and 'STORE' push-button as required (for control functions refer to Sections 3.5.4 and 3.5.3).

(6) The measurement may be conducted on FREQUENCY or PERIOD function; the two functions are treated separately below.

(a) Frequency Function:

When the 'FREQ A' push-button is depressed, signals (of frequency f_S) applied to the 'STD' socket pass by way of a frequency divider chain to the gate control circuit. The gate is held open while a number of pulses, equal to the division factor of the chain, is received at the 'STD' socket; the division factor is indicated by the setting of

the range switch (blue scale: 1 to 10^7 in decade steps). Throughout the gating period, signals (of frequency f_A) applied to the 'A INPUT' socket pass through the gate to the counter/indicator-drive circuits.

$$\text{The Displayed Count} = \frac{f_A}{f_S} \times \text{Division Factor}$$

The ratio $f_S : f_A$ is therefore given by:

$$\frac{\text{Division Factor}}{\text{Count}} : 1$$

Example

With the 'FREQ A' push-button depressed, the range switch set to 10^4, f_S = 80kHz, f_A = 20kHz and a displayed count of 2500 the ratio f_S to F_A would be given by:

$$\frac{10^4}{2500} : 1$$

$$= 4 : 1$$

(b) Period Function:

While the 'PERIOD' push-button is depressed the gate is controlled by signals (of frequency f_A) applied at the 'A INPUT' socket. These signals pass by way of a divider chain to the gate control circuit; the gate is held open while a number of pulses, equal to the division factor of the chain, is received at the 'A INPUT' socket. The division factor is indicated by the setting of the range switch (blue scale: 1 to 10^7 in decade steps). Throughout the gating time, signals (of frequency f_s) applied to the 'STD' socket pass through the gate to the counter/indicator-drive circuits.

$$\text{The Displayed Count} = \frac{f_s}{f_A} \times \text{Division Factor}$$

The ratio $f_s : f_A$ is therefore given by:

$$\frac{\text{Count}}{\text{Division Factor}} : 1$$

Example

With the 'PERIOD' push-button depressed, the range switch set to 10^3, f_S = 80kHz, f_A = 20kHz and a displayed count of 4000 the ratio of f_S to f_A would be given by:

$$\frac{4000}{10^3} : 1$$

$$= 4 : 1$$

NOTE For either function 'a' or 'b' above, the range switch setting should be such that the count capacity is not exceeded. For maximum accuracy the displayed count should be the highest obtainable without exceeding the count capacity.

(7) Momentarily depress the 'RESET' push-button

(8) Adjust the setting of the 'TRIGGER LEVEL' control to suit the signal waveform applied at the 'A INPUT' socket (for control use refer to Section 3.5.2).

3.11 DATA OUTPUT FACILITY

This facility is an optional extra that is provided only if specifically requested when the instrument is ordered. For this facility either of two options may be ordered: serial output (Option Y) or parallel output (Option Z). The particular form of output provided is denoted by the corresponding suffix 'Y' or 'Z' which is added to the instrument type reference on the rear panel label.

The data is presented at an Amphenol 36-pin socket mounted on the rear panel. Each digit is presented in b.c.d 1-2-4-2 code (for signal specification refer to Section 2.5.7).

NOTE The data outputs are obtained from the count-storage circuits; therefore, with the 'STORE' push-button depressed the recording time of data logging equipment may extend up to the end of the subsequent gating period. When the 'STORE' push-button is in the released condition the recording time must not exceed the minimum display time of the instrument; this restriction ensures that data logging will be completed before the instrument is reset.

Connections at the output socket are as follows.

NOTE MSD = Most significant digit
LSD = Least significant digit

Option Y (Serial Output):

Pin	Function
1	BCD 1
2	BCD 2
3	BCD 4
4	BCD 8
5	Clock Signal
10	Sequence Start Signal
35	Print/Punch Command O/P
36	Chassis-earth

Other pins unused

Option Z (Parallel Output):

Pin No.	Function	Pin No.	Function
1	MSD Line 1	19	4th MSD Line 8
2	MSD Line 2	20	Unused
3	MSD Line 4	21	5th MSD Line 1
4	MSD Line 8	22	5th MSD Line 2
5	Unused	23	5th MSD Line 4
6	2nd MSD Line 1	24	5th MSD Line 8
7	2nd MSD Line 2	25	Unused
8	2nd MSD Line 4	26	6th MSD Line 1
9	2nd MSD Line 8	27	6th MSD Line 2
10	Unused	28	6th MSD Line 4
11	3rd MSD Line 1	29	6th MSD Line 8
12	3rd MSD Line 2	30	Unused
13	3rd MSD Line 4	31	LSD Line 1
14	3rd MSD Line 8	32	LSD Line 2
15	Unused	33	LSD Line 4
16	4th MSD Line 1	34	LSD Line 8
17	4th MSD Line 2	35	Print/Punch Command O/P
18	4th MSD Line 4	36	Chassis-earth

Section 4	MAINTENANCE

4.1 CASE REMOVAL

WARNING Whenever the instrument is operated with the case removed, ensure that no physical contact is made with exposed connections of the mains supply circuit (particularly the tags of the mains transformer) and the exposed connection of the internal +240V d.c. supply indicated on layout diagram S69/84.

The instrument case is in two sections each secured by two fixing screws at either side of the unit. Removal of the top section gives access to the power unit and vertically mounted plug-in printed circuit boards and their preset controls; removal of the lower section gives access to the socket pins of the plug-in boards and to the preset control (R16) of the front panel switch assembly.

4.2 FUSE

A cartridge fuse, connected in the LIVE line of the mains input circuit, is housed in a screw type container accessible above the mains cable entry in the rear panel. The appropriate fuse rating depends upon the supply voltage:

Supply Voltage	Fuse Rating	Venner Part Number
100-125V	600mA slow blow	Z52053/4
200-250V	300mA slow blow	Z52053/1

4.3 PLUG-IN MODULE COMPLEMENT

In the following table the colour code refers to the colours of the finger-grip/spacers that are fitted at the top of certain plug-in printed circuit cards: colours marked on the chassis beside the corresponding sockets indicate the appropriate card positions.

Type	Title	Colour Code	Quantity
77/010	Front Panel Assembly	-	1
77/020	Rear Panel Assembly	-	1
77/220	Power Supply	-	1
77/300	Pre-Amplifier	-	1
77/310	Pulse Shaper	Red	1
77/320	Start/Stop Shapers	Pink	1
77/400	Divider Interface	Grey	1
77/500	Oscillator and Divider	Green	1
77/600	Gate Control & Reset	Beige	1
77/700	Counter	Blue	1
77/807	Display	-	1
77/817	Display Control	-	1

NOTE In instruments carrying an optional facility a plug-in card is substituted or added as indicated below.

Option Ref.

K : Card type 77/511 Oscillator and Divider (Green) fitted in place of card type 77/500.

L : Card type 77/510 Oscillator and Divider (Green) fitted in place of card type 77/500.

Y : Card type 77/910 Serial BCD Interface added.

Z : Card type 77/900 Parallel BCD Interface added.

The positions of the various plug-in modules are indicated in layout diagram S69/84.

4.4 PRESET D.C. SUPPLIES — ADJUSTMENT

Power unit type 77/220* provides three stabilized low tension supplies for the semiconductor circuits, and one unstabilized high tension supply for the digital indicator tubes.

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* For location refer to layout diagram S69/84

The three low tension supplies may be monitored at the socket that houses plug-in card type 77/320* (colour coded PINK). The voltage range, monitoring pin and (where applicable) the control at which voltage adjustment may be made are listed below for each low tension supply.

Low Tension Supply	Monitoring Pin (77/320 Socket)	Voltage Adjustment Control (on Power Unit)
+5V $^{+}_{-}$0.25V	Pin 1	-
+13V $^{+0.2V}_{-0V}$	" 3	R2*
-16V $^{+0V}_{-0.2V}$	" 4	R3*

NOTE
1. Pin 2 (77/320 socket) is the OV or common line of the three supplies
2. Recommended voltmeter: Universal AVO Meter Model 8
3. Observe meter range and supply polarity when connecting voltmeter.

The high tension supply (+240V $^{+}_{-}$15V) may be monitored between the CHASSIS-EARTH tag secured to the top of Pre-Amplifier type 77/300 (voltmeter negative) and the 'H.T. TEST POINT' (positive end of power unit capacitor C1): both connection points are indicated on layout diagram S69/84.

4.5 PULSE SHAPER PRESET CONTROL — ADJUSTMENT

NOTE The instrument supply should be switched on for a stabilization period of at least five minutes prior to control adjustment.

The plug-in Pulse Shaper card type 77/310 carries one preset control: potentiometer R2. The control may be adjusted by means of a screwdriver or trimmer tool, which may be inserted through a small hole in the right hand side plate of the instrument when the case has been removed (for hole location refer to layout diagram S69/84).

To adjust the control proceed as follows.

(1) Check that the knob of the 'TRIGGER LEVEL' control is secured on its spindle such that the angular rotation available in clockwise and anti-clockwise directions about the centre mark (excluding the additional angular rotation for operation of the 'L.F.' switch) are equal.

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* For location refer to layout diagram S69/84.

If necessary re-position and secure the knob: for knob removal refer to Section 4.8.2.

(2) Set the rear-mounted 'STD' switch to 'INT', depress the 'FREQ.' push-button and set the range switch to '10^5'

(3) Apply a standard frequency sinusoidal 1kHz 10mV r.m.s. signal to the coaxial 'A INPUT' socket.

(4) Set the 'DISPLAY TIMER' to 'MIN.' and momentarily depress the 'RESET' push-button.
At this juncture the 'GATE OPEN' neon lamp should be flashing; indicating a fast and consistent cyclical gating action.

(5) Set the 'TRIGGER LEVEL' control to the middle position and set the adjacent slope switch to '∿'

(6) Slowly turn Pulse Shaper potentiometer R2 clockwise and then anti-clockwise while observing the display. A recurrent display of 00001.00 should be obtainable between two settings of the control. The control may be turned in either direction several times until the two positions are determined; then set the control midway between these two positions.

(7) Slowly turn the 'TRIGGER LEVEL' control anti-clockwise while observing the display. At first the display should be 00001.00 but a position should be reached for which the display changes to zero; note this position of the control. Now slowly turn the control clockwise, the display should revert to 00001.00 but beyond the centre mark a position should be reached for which the display changes to 00000.01; note this position. The two noted control-positions should be approximately equi-distant about the centre mark on the panel. If necessary R2 may be re-adjusted to obtain the required performance of the 'TRIGGER LEVEL' control.

4.6 OSCILLATOR PRESET CONTROL — ADJUSTMENT

NOTE The instrument supply should be switched on for a stabilization period of at least fifteen minutes prior to control adjustment.

Plug-in Oscillator cards type 77/500 (standard) and 77/511 (option 'K') carry a preset trimmer control mounted on the side farthest from the power unit*.

On card type 77/511 the control is contained in a can unit with a small hole in the top giving access for a trimmer tool.

In instruments fitted with option 'L' the trimmer control is housed in the oven unit, which is mounted in front of the power unit*. A small hole in the top of the oven unit gives access for a trimmer tool.

To adjust the preset trimmer proceed as follows.

(1) Set the rear-mounted 'STD' switch to 'INT'., depress the 'FREQ. A' push-button and set the range switch to '1' and the 'DISPLAY TIMER' to 'INF'.

(2) Connect one beam of a double-beam oscilloscope between the 'TEST 1MHz' output socket and chassis, and the second beam to a standard frequency source providing 1MHz signals of amplitude suitable for oscilloscope display.

(3) Set the oscilloscope so that it is triggered by signals from the standard frequency source.

(4) Compare the oscilloscope traces and, by use of a suitable trimmer tool, adjust the setting of the trimmer until the frequency of the 'TEST 1MHz' signal is identical to that of the standard frequency signal.

NOTE If the 'TEST 1MHz' frequency changes as the tool is removed re-adjust the control, allowing for the effect of tool capacitance, so that the two signals are identical in frequency when the tool has been removed.

(5) Allow several minutes to elapse for oscillator stabilization, then check that no drift in oscillator frequency has occurred; if necessary repeat the procedure from (4) above.

4.7 PRESET DISPLAY DIMMING CONTROL — ADJUSTMENT

The purpose of the display dimming circuit is treated in the 'Note' appearing in Section 3.5.4. The action of the circuit is controlled by a preset potentiometer that is mounted on the underside of the Front Panel Assembly board type 77/010*: the control, which is situated near the rear of the 'RESET' push-button, is accessible for adjustment from beneath the instrument when the lower section of the case has been removed.

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* Refer to layout diagram S69/84

To adjust the preset control proceed as follows.

(1) Set the range switch to '1'

(2) Simultaneously depress push-buttons 'FREQ.' and 'PERIOD' (both push-buttons should remain locked in the depressed position).

(3) By use of a small screwdriver turn the preset potentiometer (R16 of card type 77/010) fully clockwise: the display should now be dim.

(4) Slowly turn the potentiometer anti-clockwise until the position is reached for which the display reverts to normal brightness; then turn the control back (clockwise) through approximately 30° (the display should now be dim).

(5) Release the two depressed push-buttons: the display should revert to normal brightness.

(6) The display should dim when the push-buttons of each pair listed below are depressed.

'PERIOD' and 'TIMING A → A'

'TIMING A→A' and 'TIMING B→C'

'TIMING B→C' and 'COUNT'

(7) Set the range switch to the extreme anti-clockwise position and depress the 'PERIOD' push-button: the display should again become dim.

4.8 DISMANTLEMENT

WARNING Switch off the supply and disconnect the supply cable before commencing to dismantle the instrument.

Dismantlement of the instrument to give maximum access to the modules and their components is treated below: for Case Removal refer to Section 4.1.

4.8.1 Plug-in Cards

Each vertically mounted plug-in card that bears coloured finger-grip/spacers, may be withdrawn by simply holding it at either end and gently pulling it upwards away from the chassis.

The vertically mounted board type 77/817* may be withdrawn(from its socket on board type 77/807)in a similar manner.

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* Refer to layout diagram S69/84

In instruments fitted with data output facility an additional plug-in card (type 77/910 for option 'Y'; type 77/900 for option 'Z') is mounted beside the supply switch push-rod. It may be unplugged and withdrawn from the top of the instrument when the two countersunk screws with spacers and nuts, which secure it to the adjacent side plate of the instrument, have been removed.

4.8.2 Removal of Front Panel, Display Board and Pre-Amplifier

(1) Remove the three control knobs.
Each control knob is secured by a screw driven through the top of the knob and into the end of its spindle: the screw head is covered by a cap that may be pulled out by means of the finger nails or a thin bladed implement.

NOTE When the knob is later refitted refer to Section 4.5(1) for the necessary position.

(2) Withdraw the four panel-fixing screws (one near each corner of the panel) and remove the front panel.

(3) Withdraw the two sub-panel fixing screws that normally lie approximately below the front panel legends 'A INPUT' and 'TRIGGER LEVEL'.

(4) Pull forward the sub-front panel with its surround,until the assembly is unplugged from the main chassis-unit. The horizontally mounted Display Board type 77/807 (housing the indicator tubes, and socket for the vertically mounting Display Control board type 77/817) may now be unplugged from its socket.

(5) Remove the screw that secures an earth-lead to the top of the Pre-Amplifier unit type 77/300*; then unplug the unit by pulling it upwards from the main chassis-unit.

NOTE For correct performance of the unit it is essential that the earth-lead be re-connected when the instrument is re-assembled.

4.8.3 Rear Panel Removal

Withdraw the four rear-panel fixing screws and pull back the rear panel assembly until it is unplugged from the main chassis-unit.

* Refer to layout diagram S69/84

4.8.4 Power Unit Removal

NOTE Removal of the Power Unit necessitates the disconnection of a number of soldered leads; therefore, removal of the unit should be effected only when it is essential. When the unit is refitted the lead connections should be carefully checked prior to switching on the supply.

(1) Ensure that the instrument has been disconnected from the supply.

(2) Locate the socket that receives the rear panel assembly: unsolder the BROWN lead (supply input wire) from socket-pin 1, and the BLUE lead (supply-input wire) from socket-pin 3.

(3) Locate the socket that receives the Display Board type 77/807: unsolder the power unit H.T. lead from socket-pin 5, and the chassis-earth lead from socket-pin 2.

(4) Four leads from the power unit are terminated on the adjacent socket that houses card type 77/320*. Unsolder these leads; the lead colours and pin-connections are given below.

Power Unit Lead Colour/s		77/320 socket Pin No.
Black/white	(+5V line)	1
Black	(OV ")	2
Blue/Black	(+13V ")	3
Violet/Black	(-16V ")	4

(5) The power unit may be removed when the four screws that secure it to the main chassis-unit have been withdrawn: these screws are accessible from the underside of the instrument.

* Refer to layout diagram S69/84

Section 5	CIRCUIT DESCRIPTION

5.1 CIRCUIT DIAGRAMS AND NOMENCLATURE

The circuit of the instrument is covered primarily by two main diagrams: a Block Schematic diagram (E69/26) showing the general system by which function selection is controlled within the instrument, and a Signal Path Diagram (E69/25) showing the various signal lines inter-connecting the plug-in cards. Separate circuit diagrams are provided for the individual plug-in cards and sub-assemblies; these are treated as and when appropriate throughout the circuit description.

Certain plug-in cards include multi-element integrated circuits. On circuit diagrams certain elements are depicted as D-shaped symbols containing the component reference of the particular integrated circuit to which they belong. Within this circuit description such elements are distinguished from others of the same integrated circuit by means of their output connection numbers which appear bracketed and as suffixes to the component reference of the 'parent' integrated circuit. Diagram E69/02 will be used to exemplify this nomenclature: two integrated circuits appear near the foot of the diagram, the lower one would be referred to as X4(8) and that above as X4(6).

When an integrated circuit element is a Schmitt trigger stage, the letters 'ST' appear inside the symbol and the integrated circuit reference number appears outside. Such marking appears on diagram E69/02.

Circuit logic levels '0' and '1' are treated in Section 5.12.

5.2 SUPPLY INPUT CIRCUIT

Diagram E68/93 shows the circuit of the rear-panel-mounted components.

The input connections of the supply cable are depicted by the points L (live), N (neutral) and E (chassis-earth). The supply passes via the double-pole push-button-operated POWER switch S1, fuse FS1 and the suppressor circuit comprising L1,2/C1 a-c. This circuit arrangement is again depicted on diagram E69/25; the supply is applied to the POWER SUPPLY UNIT type 77/220, the full circuit of which is shown on diagram E68/92.

The mains supply is received at transformer T1, the primary windings of which should have been appropriately linked to suit the supply voltage: series connected for 200-250V a.c. or parallel connected for 100-125V a.c.*

* For transformer connection refer to Section 3.1

Three low tension stabilized supplies are produced by the power unit: (i) +5V* available at pin 9 and derived via full-wave rectifying diodes D3,4 and integrated circuit X2; (ii) +13V* available at pin 6, preset by control R2 and derived via D2, 5 and X1; (iii) -16V* available at pin 7, preset by R3 and derived via D7,8 and X3.

One unstabilized high tension supply of +240V* is produced by the unit. This supply is available at pin 1; it is derived via full-wave rectifying diodes D1,6 and smoothed by the action of C1.

The common line of the four supplies (OV: chassis-earth) is connected to pin A.

The five output lines of the power unit are represented on diagram E69/25, but the individual connections of these supply lines to the various modules or sub-circuits of the instrument are indicated on diagram E69/26.

5.3 FUNCTION SELECTION CIRCUIT

The instrument employs a number of signal gates that are housed by various plug-in cards and are opened (enabled) or closed (inhibited) in different combinations according to the function that is to be performed.

Whether a gate is enabled or inhibited is determined by the potential applied to its control input/s.

The arrangement of control lines of the plug-in cards is shown on diagram E69/26. The control lines stem from the SWITCH BOARD ASSEMBLY AND FRONT PANEL circuit type 77/010, which is shown in full on diagram E68/91.

On this diagram E68/91 the function selector push-buttons appear as switches S7(A-D) to S11(A to D) and are shown in the 'rest' or 'out' positions.

When FREQUENCY function is selected the 4-pole switch S7(A-D) changes state so that the +13V potential (received at termination 3) is applied to the control lines connected to terminations R,N and T. The potential is also applied to the rotor of RANGE switch wafer S1C; on certain settings of the switch it serves to actuate the appropriate decimal point in the display by way of termination 21,22 or 24. The rotors of wafers S1A and S1B are strapped to the +13V supply line: S1A controls frequency division within the instrument, and S1B controls divider transfer action within the circuit of the oscillator card.

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* With respect to chassis-earth; for voltage tolerance refer to Section 4.4

Similar action occurs when each of the remaining function selector push-buttons are separately depressed to establish the particular gating combination appropriate to the required function.

The circuit of TR1, which includes R(2-6),13 and 14 as current weighting resistors, serves to detect whether more than one function selector push-button is depressed at any one time,or whether position 1 of RANGE switch S1 is selected on PERIOD function.

For either eventuality a positive-going potential change is produced at termination 18: by cut-off of TR1-collector current and conduction by D2 (when more than one function selector push-button is depressed) or by termination of R13 and R14 to the +13V supply line for cut-off of D2 diode current and override of T1 (when RANGE switch position 1 is selected on PERIOD function). The potential change serves to trigger the scan alarm circuit by way of card type 77/807 so that the display is dimmed to indicate an incorrect setting of the controls.

The complement of the main gating waveform (represented thus: $\overline{\text{GATE CONTROL O/P}}$) is received at termination 11 and operates the circuit of TR2 and neon lamp LP1: when the gate is open TR2 collector current is cut-off and LP1 is illuminated until, at the end of the gating period, TR2 again conducts.

The lines from terminations 15 and 16 convey the 10MHz and 1MHz test outputs of cards types 77/500 and 77/400 to output sockets SK1 and SK2.

A monostable circuit, which determines the time for which displays are retained, is carried by card type 77/600 and is connected by way of termination F to the DISPLAY TIME ganged controls R19 and S2. When switch S2 is closed R19-slider is connected to the OV line (at termination 2): the setting of R19 then determines the monostable period and, therefore, the display time. When S2 is open R19-slider is connected to the mid-point of potential divider R1/R12; for this condition the monostable is held inoperative and each display is retained until reset action is initiated by momentary depression of RESET push-button S3.

Depression of S3 connects the reset line of card type 77/600 (received at termination H) to the OV line (received at termination 2). Similarly when the STORE push-button is depressed the STORE control line of card type 77/400 (received at termination M) is connected to the OV line.

For functions 'TIMING B→C' and 'COUNT A/B→C' the +3V line is connected, by way of S10B and S11B, to termination L (for application to card type 77/320 control input 13) and to the rotors of START and STOP switches S5 and S6. Depression of S5 applies the +13V potential to the START control

line of card type 77/600, and depression of S6 applies the +13V potential to the STOP control line of the same card.

5.4 PRE-AMPLIFIER TYPE 77/300 (Diagram E69/95)

The 'A INPUT' socket shown on diagram E95/25 is socket SK1 of the Pre-Amplifier circuit shown on diagram E69/95.

Signals received at the socket pass to the input network in which C1 acts as coupling capacitor and R5/C4 provide compensated ballast for clipping diodes D1 and D2.

When the SLOPE switch S2(A,B) is set to either of the pulse positions ('+' or '-') components C12/R6,21 combine with R5 and C4 to form an input attenuator: the attenuation factor of which is approximately 5.

When the TRIGGER LEVEL control is turned fully clockwise its ganged switch S1 brings C5 into circuit to establish low pass filter action.

The clipping diodes D1 and D2 serve to confine the amplitude of signals, passed to the gate of a.c.-coupled transistor TR1, to within ±1V.

A trigger level control voltage for the gate circuit of TR1 is derived from the +13V supply by the potential divider comprising R2 and preset potentiometer R1.

At junction R7-C7 the trigger level control voltage combines with feedback, received at termination 6, from the subsequent Pulse Shaper card. The trigger level control circuit is such that movement of R1-slider from mid-position to either end of its track should cause the d.c. output level of the pre-amplifier, at termination 3, to change by approximately ±1V.

The pre-amplifier comprises TR1 as source follower and TR2/TR3 arranged as a two-stage compound negative feedback amplifier. The d.c. gain of the pre-amplifier is set to approximately 10 by means of R14,R15 and R17. The overall gain for either pulse input setting of S2 is approximately 1.5.

On the sinewave position of the SLOPE switch series connected components R16-C10 are switched in parallel with R14 by S2A; the pre-amplifier overall a.c.-gain is then approximately 25.

Section S2B of the SLOPE switch controls the slope selection circuits of the 'PULSE SHAPER' plug-in card type 77/310.

5.5 PULSE SHAPER TYPE 77/310 (Diagram E68/94)

Feedback Amplifier:

Output signals of the PRE-AMPLIFIER type 77/300 are received at termination 16.

The circuit of TR1 functions as d.c. bias feedback amplifier and employs R1/C1 and R5/C2,3 as signal integrators; its output passes via termination 15 to the pre-amplifier (termination 6) described in Section 5.4. The feedback voltage from the amplifier is adjustable by means of R2, the setting of which is treated in Section 4.5.

Shaper Circuit:

Signals received at termination 16 feed the circuit of p-n-p transistor TR2 which serves as input buffer/emitter follower, and temperature compensates the base circuit of TR3 for stability of the pulse shaper trigger level threshold.

The pulse shaper consists primarily of TR3/TR4 in a configuration similar to that of a Schmitt trigger circuit but with the two transistors directly coupled for high speed operation. Diode D3 permits the collector voltage of TR3 to swing positive by approximately 1.5V without attenuation of TR3 emitter current. The low value of common emitter resistor R12 enables the threshold differential of the trigger circuit to lie within the range approximately 300 to 400mV.

The pulse shaper output from TR4-collector drives emitter follower TR5, which acts as buffer and interfacer for the subsequent slope selection circuit.

Slope Selection Circuit:

This circuit consists essentially of integrated circuit X1 which comprises four two-input NAND-gates. The NAND-gates X1(6)* and X1(11) are employed in twin circuits each with a control input (terminations 14 and 13); NAND-gate X1(11) receives the output of TR5 directly, while the other receives it by way of inverter X1(3). The twin NAND-gate circuits feed X1(8) at whose output either 'true' or 'false' signals, derived from TR5, are produced. The 'true' output occurs while termination 14 is connected to chassis-earth; the 'false' output occurs when termination 13 is connected to chassis-earth. The connection to chassis-earth of the appropriate control termination is performed by switch section S2B of the pre-amplifier circuit referred to in Section 5.5.

Output signals of NAND-gate X1(8) feed the circuit of TR6/TR7 which forms a low frequency output stage for signals derived from the shaper

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* For nomenclature refer to Section 5.1

circuit and used on functions PERIOD and TIMING. Throughout the instrument resetting period, TR7 is held cut-off to inhibit the production of output signals at termination 6.

Output signals of NAND-gate X1(8) also feed the gating circuit of quadruple NAND-gate integrated circuit X2. The signals are received at X2(3) input 1 but this NAND-gate together with X2(11) are enabled, by means of control input termination 8, only for the functions FREQUENCY and COUNT A/B→C. When either function is used termination 10 is held at approximately +5V so that X2(8) is 'enabled' to permit signals, received at termination 7, to pass to X2(6) input 5 where they serve to gate the output of X2(3).

For functions PERIOD and TIMING, termination 8 is held at OV to 'inhibit' X2(3) and X2(11) whose outputs for this condition hold X2(6) and X2(8) 'enabled'; therefore, signals received at termination 10 pass via X2(8) and X2(6) to gated output termination 5.

The various signal lines to and from the pulse shaper card are represented on SIGNAL PATH DIAGRAM E69/25.

5.6 OSCILLATOR AND DIVIDER TYPES 77/500, 510 and 511

Reference signals for the various time dependent measurements conducted by the instrument are produced by the plug-in OSCILLATOR AND DIVIDER card. Within the standard instrument this card is type 77/500; for option 'L' it is replaced by card type 77/510 whilst for option 'K' it is replaced by card type 77/511.

Section 5.6.1 is applicable to the standard instrument; Section 5.6.2 is applicable to instruments carrying either of the two options.

5.6.1 Oscillator and Divider Type 77/500 (Diagram E69/02)

Oscillator and External Input Circuit:

The oscillator section of this card contains transistors TR3 and TR4 which are connected to form a crystal controlled oscillator.

Transistor TR3, operating in common base mode, drives emitter follower TR4. Feedback to the circuit of crystal XL1 is obtained from the split emitter load R23/R24 of TR4. The frequency of oscillation is preset to 10MHz by trimmer capacitor C8, adjustment of which is treated in Section 4.6.

The oscillator output from TR4-collector feeds input 9 of integrated circuit X3(8) by way of the interfacing circuit D7/R25. The integrated circuit comprises a Schmitt trigger stage which functions as

shaper for the oscillator output; however, the stage is held inoperative while termination N is connected to chassis-earth which is the condition established when the 'STD' switch is set to the 'EXT' (external) position, as shown on SIGNAL PATH DIAGRAM E69/25.

Signals received at the 'STD' external reference input socket (SK4 on diagram E69/25) are accepted at termination 11 of the card (diagram E69/02). The signals pass to the a.c.-coupled common emitter amplifier TR2 for which D6 functions as clipping diode for negative excursions of the waveform; positive excursion clipping is provided by the TR2 base-emitter junction and capacitors C4/C5.

The collector output of TR2 feeds input 5 of integrated circuit Schmitt-trigger/pulse-shaper stage X3(6). This stage is held inoperative while termination P is connected to chassis-earth: the condition established when the 'STD' switch is set to 'INT'.

The outputs of pulse shapers X3(8) and X3(6) feed NAND-gate X4(3). The setting of the 'STD' switch determines which pulse shaper shall be operative and which inoperative: it thus determines from which source (internal or external) the reference signals shall be derived. The output potential of the inoperative shaper is such as to hold X4(3) 'enabled' for the passage of the required signals.

Output signals of X4(3) feed the 10MHz test socket of the instrument by way of R31 and termination R; they also feed input 4 of NAND-gate X4(6) and, while this stage is 'enabled' by the control potential at termination 16, pass via inverter/NAND-gate X4(8) to the oscillator (internal or external) output termination T.

Throughout the resetting period of the instrument the control potential at termination 16 is such as to inhibit X4(6) so that no reference signal pulses occur at termination T until reset action has been completed.

Divider Circuit:

The divider circuit comprises the large scale integrated circuits X1 and X2 and their associated components.

Each integrated circuit contains two pairs of cascade-connected decades. The first pair: input 4, output 8. The second pair: input 14, output 9 . The four pairs are linked, as shown on diagram E69/02, to form a chain of eight cascade-connected decades. The chain is fed by signals received at termination 7.

By means of the potentials on control lines at terminations L,M,9 10 and 6 any one of the decades may be selected to supply its output, via connection 2 and inverter/amplifier TR1, to termination J. Each control line is either connected to the +13V supply line or left in the open circuit state by the rotary RANGE switch S1(A-D) of diagram E68/91 treated in Section 5.3.

Decade reset action is controlled by the circuit containing diodes D1-5. A positive-going reset pulse received at termination H resets each decade to the nine state when diode gate D1/D2 is 'enabled' by a +13V potential at termination E, or to the zero state when diode gate D3/D4 is 'enabled' by a +13V potential at termination F.

The circuit of TR5 serves to hold connection 5 of X1 and X2 at approximately OV for part of the reset period: a condition necessary to achieve fast reset action of the decade chain.

5.6.2 Oscillator and Divider Types 77/510 and 77/511 (Drg. E69/22)

The circuit shown on diagram E69/22 covers cards type 77/510 and 77/511 and, with the exception of the oscillator stage feeding input 9 of integrated circuit X3, is identical to the circuit of card type 77/500 described in Section 5.6.1.

Two oscillator stages enclosed by chain lines and marked 'A' and 'B' appear on diagram E69/22. Only one of these stages is included in the circuit: stage 'A' for card type 77/511, stage 'B' for card type 77/510.

Stage 'A' is the temperature compensated 10MHz sinewave crystal oscillator (card type 77/511: option 'K'*). Stage 'B' is the oven controlled 10MHz sinewave crystal oscillator (card type 77/510: option 'L'*) for which the oven supply is received by way of connectors SK2 and PL2.

Both oscillator stages incorporate a trimmer capacitor, adjustment of which is treated in Section 4.6.

5.7 DIVIDER INTERFACE TYPE 77/400 (Drg. E68/100)

This plug-in card houses several signal level interfacing circuits for inter-connection of a number of circuit-sections of the instrument; it also carries several subsidiary gating circuits which enable the passage of signals to be inhibited for certain functions of the instrument.

* Refer to Section 2.5.4

Pulses produced at output termination T of the OSCILLATOR AND DIVIDER card (and derived from the 10MHz internal oscillator or from an external reference source) are received at termination T (drg. E68/100). These signals take two routes:

(i) They pass by way of X1(11) when this NAND-gate is 'enabled' on functions FREQUENCY and COUNT (by means of control termination M) or PERIOD (by means of control termination K). For each of these three functions the signals feed input 2 of X3(3): on other functions the output level of X1(11) holds X3(3) 'enabled'.

(ii) They are inverted by X1(3) and, while X1(6) is 'enabled' by control termination 15, pass to input 9 of X1(8). NAND-gate X1(8) is 'enabled' on both TIMING functions, by control termination L, so that the signals feed input 1 of X3(3): on other functions the output level of X1(8) holds X3(3) 'enabled'.

Output pulses of X3(3) drive integrated circuit decade X2 for which reset signals are received at termination N. Output pulses of the decade, which occur at one tenth of the input pulse rate, feed the 1MHz test socket of the instrument by way of inverter X3(6).

By means of control terminations L and M the base of TR6 is biased positive for all functions except PERIOD, to allow the output pulses of decade X2 to operate TR6 for the production of corresponding pulses (swinging between the levels approximately OV and +12V) at TR6-collector.

On PERIOD function TR6 is 'inhibited' but the diode gate D12/D14 is 'enabled', by control termination K, so that pulses (from the L.F. output of pulse shaper type 77/310 treated in Section 5.5) received at termination 9 may operate TR7 for the production of corresponding pulses at TR7-collector.

Pulses produced at the common collector junction of TR6/TR7 pass by way of termination 7 to the multi-decade divider chain, treated in Section 5.6. The pulses also pass via diode D8 and transistor TR9 to input 13 of NAND-gate X3(11), but only when control termination 6 is held at +13V.

While no decade of the OSCILLATOR AND DIVIDER card (treated in Section 5.6) is selected, NAND-gate X3(11) is 'enabled' by means of termination J. Pulses from TR9-emitter then pass to output termination P (to feed termination 13 of the GATE CONTROL AND RESET card) and by way of inverter X3(8) and termination R to the standard frequencies output socket of the instrument.

When a decade of the OSCILLATOR AND DIVIDER card is selected,

X3(11) is held 'enabled' by TR10 for the output of the selected decade to feed terminations P and R. Transistor TR10 is cut-off when control termination 6 or 8 is held at +13V, but conducts to 'enable' X3(11) when both control terminations (6 and 8) are open circuit.

Emitter follower TR8 allows the output of X3(3) to operate X3(11) without first being frequency divided by decade X2: this can occur only when control termination 8 is held at +13V.

For PERIOD function control termination K is held at +13V so that pulses at termination 16 are produced by output signals of X1(6): for both TIMING functions control termination L is held at +13V so that the pulses at termination 16 are produced by the output of X3(11) and pass by way of D11 and TR2.

The circuit of TR4 and TR5 is employed to produce a 'STORE TRANSFER' pulse at terminations 11 and 14 but is functional only when the 'STORE' push-button (shown on diagram E69/25) is depressed to connect termination 12 to chassis-earth. The pulses are initiated upon receipt of a negative-going signal received at termination S on completion of the gating period.

The amplitude of the pulse produced at termination 11 is approximately equal to the supply voltage level (+13V), but that of the pulse produced at termination 14 is restricted to +5V by potential divider R12/R14. The two pulses serve to control the transfer of information within the COUNTER card.

5.8 STOP AND START SHAPERS TYPE 77/320 (Drg. E69/01)

Input sockets 'START' and 'STOP' (SK1 and SK2 on SIGNAL PATH DIAGRAM E69/25) are for use only on functions 'TIMING B→C' and 'COUNT', when they may be used to start and stop the main signal-gating action within the instrument. The 'START' socket feeds termination 15 and the 'STOP' socket feeds termination 11 of card type 77/320.

The circuit of the card (diagram E69/01) comprises twin amplifier/pulse-shaper circuits, one operated by 'start' input-signals the other by 'stop' input-signals.

Termination 13 serves as control line input for both circuits; when it is held open circuit the amplifier/pulse-shapers are 'inhibited'; when it is held at +13V they are 'enabled'.

Because the two circuits are identical (except for terminations) only the start circuit containing TR1-3 and X1(6) will be described.

The action of the circuit is dependent upon the setting of the rear-panel-mounted SLOPE switch connected to terminations 14 and 16. The output of the circuit occurs at termination 7 and is a positive-going pulse of approximately 0.1μs duration; this is initiated by the positive-going excursion of the input waveform when the SLOPE switch is set to '+' (termination 14 held at +13V: termination 16 open circuit) but from the negative-going excursion when the SLOPE switch is set to '-' (termination 16 held at +13V: termination 14 open-circuit).

Signals received at termination 15 pass via a.c.-coupled amplifier TR1 to input 1 (strapped to inputs 2 and 4) of integrated Schmitt trigger stage X1(6).

When the SLOPE switch is set to '+', termination 14 is held at +13V so that the bias at X1(6) input 1 is greater than +2V, and TR3 is held cut-off by current drawn via D1 and potential divider R10/R12.

For this condition the amplitude of X1(6) output pulses is not sufficient to change the state of TR3, which is a.c.-coupled by C7. However, the pulses drive inverter TR4 which feeds a.c.-coupled output transistor TR2. The differentiating action of C6/R8 ensures that for each positive-going output pulse of X1(6) a positive-going pulse (of approximately 0.1μs duration) occurs at output termination 7.

When the SLOPE switch is set to '-', termination 16 is held at +13V so that TR2 is held cut-off; the bias at input 1 of X1(6) is then approximately +0.5V.

Input pulses by way of amplifier/inverter TR1 operate the Schmitt trigger stage. Negative-going pulses at X1(6) output, differentiated by C7/R10, operate TR3 for the production of the positive-going output pulse at termination 7.

The 'start' pulse output (termination 7) feeds input termination 6 of the GATE CONTROL AND RESET card type 77/600: the 'stop' pulse output (termination 6) feeds input termination F of the same card (type 77/600).

5.9 GATE CONTROL AND RESET CIRCUIT TYPE 77/600

Plug-in card type 77/600 houses the gate control interfacing circuit, two flip-flops controlling the main gating action of the instrument, a monostable of the display timing circuit, and an inhibit timer and reset signal generator.

Interfacing and Gate Control Circuit:

Two integrated circuit JK-flip-flops X2(13) and X2(8), arranged in inter-lock connection, form the control circuit for the main gate of the instrument. The 'clock' input of both stages (inputs 1 and 5) are linked together and receive the trigger pulses that initiate gating action.

The trigger pulses are received, by way of separate interfacing circuits, from different sources according to the particular function that the instrument is required to perform.

For functions FREQUENCY and PERIOD pulses received at termination 13 pass to the clock inputs of the flip-flops via NAND-gate X3(1),which is 'enabled' by a +13V potential applied to control termination 7.

When function TIMING A-A is selected, pulses received at termination L pass to the flip-flop clock inputs via NAND-gate X3(4) held 'enabled' by +13V at control termination J.

On functions TIMING B-C and COUNT the 'start pulse', received at termination 6 (and produced by the start pulse shaper of card type 77/320) or received at termination 11 (and produced by depression of the START push-button shown on diagram E69/25), feeds the clock inputs of the flip-flops by way of X3(10). A similar circuit, that of X3(13), receives the 'stop pulse' via termination F or 12. During the inhibit period of the instrument start pulse NAND-gate X3(10) is 'inhibited' by means of the potential produced at termination 16 which then holds TR6 conductive.

After a reset pulse has been received at the clear inputs of the flip-flops the logic levels at the outputs are: '0' at the Q output of flip-flop X2 (13); '1' at the $\overline{Q}$ output of flip-flops X2 (13) and X2 (8).

The flip-flops having thus been reset, the first negative-going pulse (the 'start' pulse) received at their common clock inputs triggers X2 (13) so that the levels at its Q and $\overline{Q}$ outputs inter-change: Q becomes '1' to produce the 'gate open level' at termination 8 and 'enable' both flip-flop X2 (8) and NAND-gate X3 (13), $\overline{Q}$ becomes '0' to 'inhibit' NAND-gate X3 (10) and produce at termination 15 the 'complement of the gate open level' (which serves to cut-off TR2 of diagram E68/91 for illumination of the GATING LAMP).

The second negative-going pulse (the 'stop' pulse) received at the common clock inputs, triggers both flip-flops; the output levels of flip-flop

X2 (13) inter-change for removal of the 'gate open level' (from termination 8) and its complement (from termination 15), and the $\overline{Q}$ output of flip-flop X2(8) swings to '0' to provide a negative-going signal at termination S.

This signal serves as 'store transfer trigger signal' and, when the instrument carries the option Y data output facility, as 'print/punch command pulse'.

Both flip-flops remain insensitive to further input signals via their clock inputs as each holds the other'inhibited': X2 (13) held 'inhibited' by the $\overline{Q}$ output of X2 (8), and X2 (8) by the Q output of X2 (13).

During the operation of the flip-flops for functions TIMING B-C and COUNT, integrator C13/R29 serves to delay the 'inhibiting' feedback to NAND-gate X3 (10) so that the first trigger signal at the clock input of X2 (13) is sustained sufficiently long to permit completion of the flip-flop trigger action. Integrator C19/R32 serves to delay the 'enabling' feedback to NAND-gate X2 (13) and ensures that the initial trigger action of flip-flop X2 (13) is completed before a stop signal may be received via X3 (13).

Display Timing, Inhibit Timing and Reset Circuits:

The negative-going signal produced (at the end of the gating period) at the $\overline{Q}$ output of X2(8) triggers the display time monostable circuit containing NAND-gate X1(3), transistors TR1 and TR2, and the front-panel-mounted DISPLAY TIMER potentiometer connected to termination 9 and shown on diagram E69/25.

During the stable state of the monostable X1(3) is held 'enabled' by the emitter potential of TR2. As the circuit is triggered the output of X1(3) swings to logic level '1' which cuts-off TR1 and TR2 collector currents: diode D12 clamps input 2 of X1(3) at approximately OV.

Provided that the ganged switch of the DISPLAY TIMER potentiometer is not set to 'INF' (Infinity: switch open) C2 discharges via R4 and the potentiometer, whose setting determines the capacitor discharge time and

consequently the display time of the instrument.

Transistor TR1 becomes conductive when junction C2/R4 tends negative with respect to the emitter; therefore, TR2 conducts and X1(3) output swings to '1', thus hastening completion of C2 discharge and triggering of the inhibit monostable by way of C6/D4.

The inhibit monostable, containing NAND-gate X1(8) and transistor TR3, may also be triggered by a similar negative-going signal received via C5/D5 (and produced upon depression of the RESET push-button connected to termination 10) or received via C8/D3 upon receipt of an external reset input signal at termination R. (Note. Termination R is used only on special models of the instrument).

As the monostable is triggered, X1(8) output swings to '1' and produces a positive-going inhibit signal at termination 14 and, by means of inverter X1(6), the complement of this signal at termination 16. The change in output level of X1(8) causes TR3 to conduct and supply a negative-going pulse via C10 for momentary cut-off of TR5 and TR4 collector currents. Three pulses are thus produced: a positive-going pulse (amplitude approx. 12V) at termination H, a positive-going pulse (amplitude approx. 5V) at termination N, and a negative-going pulse (amplitude approx.2.5V) at termination P.The duration of the three pulses is approximately 25us.

At the end of the inhibit period (approx. 4ms, governed by the charging time of C9) TR3 is cut-off and its collector applies logic level '1' to input 10 of X1(8), so that the output of the NAND-gate reverts to '0' for removal of the inhibit signal and its complement from terminations 14 and 16.

5.10 COUNTER AND DISPLAY CIRCUITS TYPES 77/700,77/807 & 77/817

Pulses from the main signal gate of the instrument are received at input termination 5 of the Counter card type 77/700 (circuit diagram E68/98). The Counter is initially reset by pulses received at terminations 7 and 13.

The Counter operates in conjunction with the circuits of the Display Control card type 77/817 (diagram E68/97) and Display card type 77/807 (diagram E68/96).

The circuit arrangement of these three inter-connected cards is shown in schematic form on diagram E69/24. Each card is represented by a rectangle marked with the appropriate type number of the card. The rectangle representing card type 77/817 is shown in chain-lines, as this card is housed

in a socket mounted on card type 77/807.

Input pulses received at termination 5 of the Counter card (type 77/700) feed a chain of seven cascade-connected decades comprising one VHF counter decade and three dual MOS counter decades; on Counter circuit diagram E68/98 these, in order of progression along the chain, are TTL integrated circuit X1 (VHF or least significant digit decade) and MOS integrated circuit decade/store modules X3, X4 and X5. Interfacing, for output pulses of the TTL decade to drive the cascade-connected MOS decades, is provided by the circuit of TR1 and TR2.

Integrated circuit X2 serves as a store for count information received in bcd form (via inputs 3,6,2 and 7) from decade X1; equivalent store circuits for the other decades are contained within X3 to X5.

The potential at termination 14 controls store X2: when it is held at approximately +5V the bcd output information of X1 is present also at the output of X2 (outputs 1,14,11,8); when it is changed to approximately OV the bcd information existing at the output of X2 is sustained (store condition) and X2 is held insensitive to changes in the output information of decade X1. The store circuits of the other decades are controlled in like manner by control termination 11: the two control lines are operated simultaneously.

The store associated with any decade may be selected for its four line output to feed terminations H,J,E and F: here the count information occurs in 1-2-4-8 bcd complement form. The stores are selected by means of control lines: terminations S,R,P,N,M,L and K corresponding to the least- to most-significant decades. When termination S is held at approximately +13V the four diode gates containing D1 to D4 and D7 to D10 are 'enabled' for the information of store X2 to pass to terminations H,J,E and F. Similar circuits for the other decade stores are housed within X3 to X5.

The stores are scanned (selected in turn) by means of a pulse that progresses around a ring circuit comprising seven transistor stages, each of which effectively operates as a half-monostable circuit.

This seven-stage ring circuit, represented in schematic form on diagram E69/24 and in circuit form on diagram E68/97, is set into operation by a SCAN STARTER circuit as the instrument supply is switched on.

The SCAN STARTER circuit comprises a relaxation oscillator housed by card type 77/807 (circuit diagram E68/96) and formed by the circuit of neon-tube V1. A negative-going pulse from the oscillator passes by way of C1

(diagram E68/96) and termination 16 (diagram E68/97) and cuts-off TR1 collector current for a period determined by the time constant C1 (diagram E68/96) x R1 (diagram E68/97). For this period termination 2 (diagram E68/97) is held at approximately +13V for selection of the most-significant-digit store, and termination 1 is held at approximately +95V (by the action of Zener diode D2 of diagram E68/96) to permit display of the corresponding numeral.

Throughout the TR1 cut-off period, digit information from the selected decade store passes (in 4-line parallel b.c.d form) from terminations H,J,E and F of the Counter card type 77/700* to terminations 9,10,7 and 8 of the Display card type 77/807*. This information is received by integrated circuit X1 (diagram E68/96) which functions as b.c.d/decimal converter; its ten digit-output lines (0 to 9) feed the corresponding parallel-connected digit-cathodes of indicator tubes V2 (most significant digit tube) to V8 (least significant digit tube). Decimal point control lines for tubes V5 to V8 are provided at terminations 21 to 24**.

While termination 1 (diagram E68/97) is held at approximately +95V, TR1 conducts and neon tube V2 is 'struck' for display of the most significant digit.

Throughout the cut-off period of TR1 (diagram E68/97) transistors TR2 to TR7 are held conductive and so hold display tubes V3 to V8 (diagram E68/96) in the non-illuminated condition.

At the end of the cut-off period TR1 (diagram E68/97) conducts and a negative-going pulse passes via C2 to cut-off TR2. Thus the function of decade-store selection and display-tube illumination is passed to the second transistor of the seven stage ring circuit; therefore, the second most significant digit is momentarily displayed. In this manner all digits are in turn displayed. The pulse that is produced as the last transistor of the ring again conducts, is fed back to TR1 so that the store-scanning/display process for the seven digits is recurrent.

Transistors TR8 and TR9 serve to permit only one pulse to circulate around the ring. During the scanning of the first six digits one or another of the transistors TR1 to TR6 is non-conductive and so provides bias (via R4 or R8 or R12...) to hold TR9 conductive; TR7 is also conductive and holds TR8

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* Refer to diagram E69/24

** For decimal point selection refer to Section 5.3 and diagrams E69/26 and E68/91.

cut-off. When the sixth most significant digit has been displayed and TR6 again conducts, and provided that none of the transistors TR1 to TR5 is held non-conductive by a further pulse in the ring, TR9 base bias is automatically removed. Transistor TR9 is therefore cut-off and the circulating pulse cuts-off TR7, which in turn causes TR8 to conduct thus 'inhibiting' receipt of any further pulse from TR6 during the cycle. Subsequently the circulating pulse is passed back from TR7 to TR1, whereupon TR9 base bias is restored.

When an incorrect setting of the controls is detected (by a circuit treated in Section 5.3) termination R is held at a potential such that diode D8 conducts to hold TR9 conductive; the normal action of the scanning circuit is thus 'inhibited' and so no pulse is passed back to TR1.

The display circuit (diagram E68/96) contains ballast resistors R19 and R20. Once the scanning circuit has been set into operation, the relaxation oscillator circuit of V1 is effectively 'switched off' by the potential developed across R19/R20 as they pass the indicator tube current. However, while the ring or scanning circuit (diagram E68/97) is 'inhibited' no tube current flows via R19/R20 and so the relaxation oscillator is free to operate and delivers pulses to the ring circuit; but because the period of oscillation is much greater than the time normally taken for a pulse to circulate the ring, the frequency of illumination of each indicator tube is relatively reduced and consequently the display appears dim.

The circuits of TR8 and TR9 (diagram E68/96) are required when the instrument carries a data logging facility*. Transistor TR8 momentarily conducts to produce a negative-going 'clock signal' (or 'digit marker pulse') at termination 19 whenever the circulating pulse in the ring circuit is passed from one stage to the next.

Transistor TR9 is momentarily cut-off to produce a positive-going 'sequence start signal' (or 'scan marker pulse') at termination 4, when a negative-going potential change occurs at termination M. This change is produced as the pulse circulating in the scanning circuit (diagram E68/97) passes to TR1 at the start of each scanning cycle.

5.11 DATA OUTPUTS

Data output is an optional facility that is provided only if it has been initially ordered. Either of two types of output may be fitted:

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* Refer to Section 2.5.7

serial output (option Y) or parallel output (option Z). The circuits for the two types of output are described below.

5.11.1 Serial B.C.D. Interface Type 77/910

This interface circuit is housed by card type 77/910(diagram E69/33). It consists of four inverters TR1 to TR4 operated in parallel by the b.c.d. $\overline{1}$, $\overline{2}$, $\overline{4}$ and $\overline{8}$ output lines of the Counter card. The outputs of the interfacing circuit feed the rear-panel-mounted data logging output socket of the instrument*. The data is presented at the socket in serial form in the order most-significant-digit to least-significant-digit.

5.11.2 Parallel B.C.D. Interface Type 77/900

The parallel b.c.d interface circuit is housed by card type 77/900 and is represented on diagram E69/27. It contains four inverters TR4 to TR7, operated in parallel by the b.c.d. $\overline{1}$, $\overline{2}$, $\overline{4}$, and $\overline{8}$ output lines of the Counter card.

The inverters feed separate seven-stage integrated circuit shift registers (X1 to X4). The seven outputs of each shift register feed the rear-panel-mounted data logging output socket of the instrument*.

Operation of the four shift registers is controlled by integrated circuit X5, which contains two flip-flops externally linked for inter-lock action. This integrated circuit employs the auxiliary circuits of TR1 to TR3: the action of the interface circuit is as follows.

At the end of the gating period of the instrument a negative-going pulse (from card type 77/600 termination S) is received at termination 14 and serves to reset the inter-lock connected flip-flops of X5 and the four shift registers X1 to X4.

When the next scanning cycle is commenced, a 'scan marker pulse' (positive-going) is received at termination 16. The signal passes via inverter TR1 and triggers the flip-flop circuit; whereupon X5 output 8 swings from logic level '1' (the reset state) to logic level '0'. This logic level change 'enables' the circuit of TR2 for control of the normally conductive inverter TR3.

As the first digit of the scanning cycle is selected for display (most significant digit) a 'digit marker pulse' (negative-going) is received at termination 15. This pulse is differentiated by C2/R7-R8 and initiates

* Connections at this socket are listed in Section 3.11

momentary conduction by TR2 and consequently momentary cut-off of TR3 for the production of a positive-going pulse at TR3 collector:the pulse simultaneously clocks integrated circuits X1 to X4 so that each of the four 'bits' of the b.c.d digit information are accepted into the first stage of their respective shift registers.

The four shift registers are progressively clocked, to store the remaining six digits, as further 'digit marker pulses' are received during the scanning cycle. At the end of the cycle a second 'scan marker pulse' is received at termination 16. This pulse triggers the flip-flop circuit: a negative-going potential change occurs at outputs 3,9 and 14 (the signal feeds termination AA and serves as 'print/punch command' output signal) and output 8 swings back to logic level '1' to 'inhibit' the circuit of TR2. The flip-flop circuit is then in the locked condition and remains insensitive to further 'scan marker pulses' until, at the end of a subsequent gating period of the instrument, another negative-going pulse is received at termination 14 whereupon reset action and a new cycle are initiated within the b.c.d interface circuit.

5.12 CIRCUIT LOGIC LEVELS

Logic levels '0' and '1' as used in the foregoing circuit descriptions are defined below.

General Control Circuits (MOS circuits excluded):

Logic '0' = levels in the range 0V to +0.4V
Logic '1' = levels in the range +2.5V to +5V.

MOS Circuits:

Each MOS output is a current drive:
'1' level (short circuit to 0V line) current
range = +0.5mA to +1.5mA.
'0' is effectively an open circuit condition.

Section 6	REPAIR

6.1 SECTION INTRODUCTION

This section of the manual supplements the information and procedures given under MAINTENANCE (Section 4) and should be used in conjunction with the circuit diagrams dealt with under CIRCUIT DESCRIPTION (Section 5). The section is not an exhaustive treatment of the subject of instrument repair but outlines certain fundamental procedures for fault location and deals with a number of malfunctions that could arise in the display system.

6.2 INTERNAL SUPPLY VOLTAGES

Malfunctions of the instrument can be caused by incorrect voltages of the internal supplies; therefore, the voltages should be checked prior to investigation into specific circuit functions. Measurement and adjustment of the internal supply voltages is treated in Section 4.4.

The presence of the appropriate supplies at the various modules should also be checked. Connection of the supply lines to the modules or sub-circuits is indicated on diagram E69/26. The production of the internal supplies is treated in Section 5.2.

6.3 OSCILLATOR AND PULSE SHAPER ADJUSTMENT

When time dependent measurements involving the use of the internal oscillator are suspected of being incorrect, the oscillator frequency should be checked (and if necessary, adjusted) in accordance with Section 4.6.

When the oscillator frequency has been checked, but incorrect results are shown on functions for which signals are received by way of the 'A' input socket, the setting of the Pulse Shaper control should be checked in accordance with Section 4.5.

6.4 CONTROL LINE VOLTAGES

The functions of the instrument are internally selected by a number of control lines which may be held at either of two voltages: the particular voltage combination of these lines determines the instrument function. The voltage combinations for the various functions are shown in TABLE 2.

For each function on which a fault condition is manifested, the

TABLE 2: CONTROL LINE VOLTAGES

NOTE. Logic Code: '1' represents +13V with respect to chassis earth.
" " '0' " ≤0V " " " " "
'C' represents open-circuit decimal point line.
'-' "- Unused.

		Sub-circuit Type 77/010 Terminations (Shown on Drg. E69/26)																	
Function	Range	T	R	N	S	X	U	W	L	20	19	AA	AB	Z	Y	17	22	21	24
Freq.	MHzx10	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	C	C	C
"	1 MHz	1	1	1	0	0	0	0	0	0	1	0	0	0	0	0	C	C	C
"	10_2 "	1	1	1	0	0	0	0	0	0	0	1	0	0	0	1	C	C	1
"	10^2_3 "	1	1	1	0	0	0	0	0	0	0	0	1	0	0	1	C	1	C
"	10^3_4 "	1	1	1	0	0	0	0	0	0	0	0	0	1	0	1	1	C	C
"	10_5 kHz	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	C	C	1
"	10^5_6 "	1	1	1	0	0	0	0	0	0	0	1	0	0	0	0	C	1	C
"	10^6_7 "	1	1	1	0	0	0	0	0	0	0	0	1	0	0	0	1	C	C
"	10^7 Hz	1	1	1	0	0	0	0	0	0	0	0	0	1	0	0	C	C	C
Period	1 period*	0	1	1	1	0	0	0	0	0	1	0	0	0	0	0	C	C	1
"	10_2 "	0	1	1	1	0	0	0	0	0	0	1	0	0	0	1	C	C	1
"	10^2_3 "	0	1	1	1	0	0	0	0	0	0	0	1	0	0	1	C	C	1
"	10^3_4 "	0	1	1	1	0	0	0	0	0	0	0	0	1	0	1	C	C	1
"	10^4_5 "	0	1	1	1	0	0	0	0	0	0	0	0	0	1	1	C	C	1
"	10^5_6 "	0	1	1	1	0	0	0	0	0	0	1	0	0	0	0	C	C	1
"	10^6_7 "	0	1	1	1	0	0	0	0	0	0	0	1	0	0	0	C	C	1
"	10^7 "	0	1	1	1	0	0	0	0	0	0	0	0	1	0	0	C	C	1
Timing A-A	µs	0	0	0	0	1	1	1	0	1	0	0	0	0	0	0	C	C	C
"	1 ms	0	0	0	0	1	1	1	0	0	1	0	0	0	0	0	1	C	C
"	10_2 "	0	0	0	0	1	1	1	0	0	0	1	0	0	0	1	C	1	C
"	10^2_3 "	0	0	0	0	1	1	1	0	0	0	0	1	0	0	1	C	C	1
"	10^3_4 "	0	0	0	0	1	1	1	0	0	0	0	0	1	0	1	C	C	C
"	10^4_5 s	0	0	0	0	1	1	1	0	0	0	0	0	0	1	1	C	1	C
"	10^5_6 "	0	0	0	0	1	1	1	0	0	0	1	0	0	0	0	C	C	1
"	10^6_7 "	0	0	0	0	1	1	1	0	0	0	0	1	0	0	0	C	C	C
"	10^7 sx10	0	0	0	0	1	1	1	0	0	0	0	0	1	0	0	C	C	C
Timing B-C	µs	0	0	0	0	1	1	0	1	1	0	0	0	0	0	0	C	C	C
"	1 ms	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	1	C	C
"	10_2 "	0	0	0	0	1	1	0	1	0	0	1	0	0	0	1	C	1	C
"	10^2_3 "	0	0	0	0	1	1	0	1	0	0	0	1	0	0	1	C	C	1
"	10^3_4 "	0	0	0	0	1	1	0	1	0	0	0	0	1	0	1	C	C	C
"	10^4_5 s	0	0	0	0	1	1	0	1	0	0	0	0	0	1	1	C	1	C
"	10^5_6 "	0	0	0	0	1	1	0	1	0	0	1	0	0	0	0	C	C	1
"	10^6_7 "	0	0	0	0	1	1	0	1	0	0	0	1	0	0	0	C	C	C
"	10^7 sx10	0	0	0	0	1	1	0	1	0	0	0	0	1	0	0	C	C	C
Count	-	1	0	0	0	0	1	0	1	-	-	-	-	-	-	-	-	-	-

* The extreme anti-clockwise position 'µs' of the Range switch should not be used on Period function: refer to NOTE in Section 3.5.4.

control line voltages should be measured and checked against the corresponding voltage combination appearing in the table. This check should be carried out prior to investigation into the circuit operation of any individual module.

Sub-circuit type 77/010, referred to in TABLE 2, may be located by reference to LAYOUT DIAGRAM S69/84, and terminations at the edge-connector of this circuit by reference to BOARD LAYOUT DIAGRAM BL77/010. The control lines feed terminations of the various modules as indicated on diagram E69/26, and in some instances it may be found more convenient to measure the control line voltages at these alternative connections.

The circuit at which the control lines originate is shown on diagram E68/91 and is described in Section 5.3.

6.5 PLUG-IN CARDS

The circuits of the various plug-in cards are described in Sections 5.4 to 5.11.2. If a fault has been traced to one of these cards and the locations of the individual components of the card are required, refer to the corresponding board layout diagram, which is provided together with the circuit diagram and components list near the rear of the manual.

6.6 NO-COUNT CONDITION AND MALFUNCTIONS OF THE DISPLAY SYSTEM

It is normal for the brilliance of the display to diminish if the controls are incorrectly set: refer to the NOTE in Section 3.5.4.

If a dim display is shown for correct settings of the controls, check the setting of the display dimming potentiometer: refer to Section 4.7.

Circuits associated with display dimming are treated in Sections 5.3 (paras. 7 and 8) and 5.10.

Below are tabulated a number of fault conditions together with appropriate checks that may be made to facilitate fault location.

No Count Registered on functions FREQ., PERIOD and TIMING

Procedure:

1. Check oscillator output at 10MHz TEST socket. If correct, check setting of 'STD' switch (refer to Section 3.5.1.) and check oscillator circuit (refer to Section 5.6).
2. For functions FREQ., Period and TIMING check for presence of divider output signals at input-termination 13 of card type 77/600; if correct, proceed with following checks.

2a. Check control line voltages: refer to Section 6.4.

2b. If the fault has been manifested on Period function by use of the test facility (treated in Section 3.6) check integrated circuit X2 of card type 77/400 and its associated components: refer to Section 5.7.

2c. Check integrated circuits X1 and X2 of OSCILLATOR & DIVIDER CARD; refer to Section 5.6.

No Display Illumination

Procedure:

1. Check supplies; refer to Section 6.2. If supplies are not present check mains input fuse (refer to Section 3.2) and the stabilizer circuit of the +13V supply (refer to Section 5.2).
2. Check scanning pulse action of card type 77/817 (refer to Section 5.10). If correct, check relaxation oscillator of card type 77/807 and transistor TR1 of card type 77/817 (refer to Section 5.10).
3. Check each display tube of card type 77/807 for anode to cathode short circuit (refer to circuit diagram E68/96).

Multi-image Display by Indicator Tube/s

Possible causes.

1. Incorrect logic output of card type 77/700 caused by faulty integrated circuit (refer to Section 5.10).
2. Faulty integrated circuit decoder X1 on card type 77/807 (refer to Section 5.10).
3. Anode to cathode short circuit on any indicator tube (refer to circuit diagram E68/96).

Section 7	ILLUSTRATIONS AND COMPONENTS LISTS

COMPONENTS LISTS

In this section each components list faces the diagram/s to which it relates. Several of these components lists appear on folded sheets; therefore, it may be necessary to extend such a sheet in order to display its entire content.

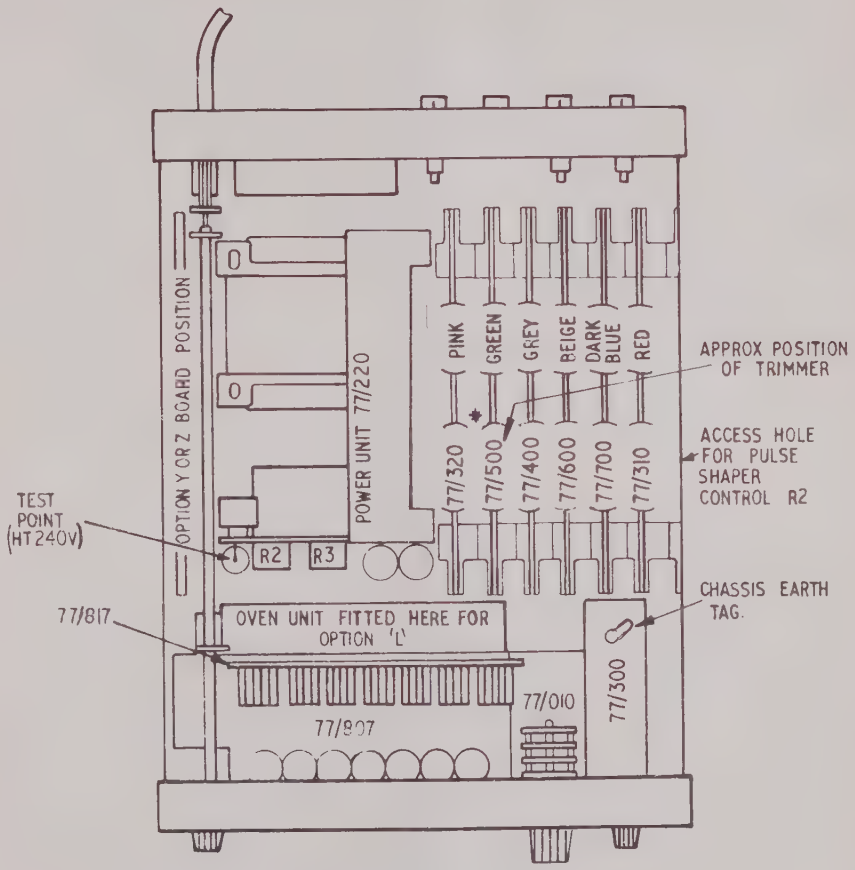
The instrument as supplied may be fitted with equivalent types of components to those stated in the subsequent lists.

BOARD LAYOUT DIAGRAMS

Illustrations showing component and copper layout of plug-in printed circuit cards are provided amongst the following diagrams.

The cards are illustrated as viewed from the non-component side; component positions appear superimposed (as though the cards were transparent).

Where a card is also copper clad on the component-side, a further illustration (below the first) shows the card as viewed from the component side but void of components (unless the board carries components on both sides; then the components shown in this view are those mounted on the reverse side).



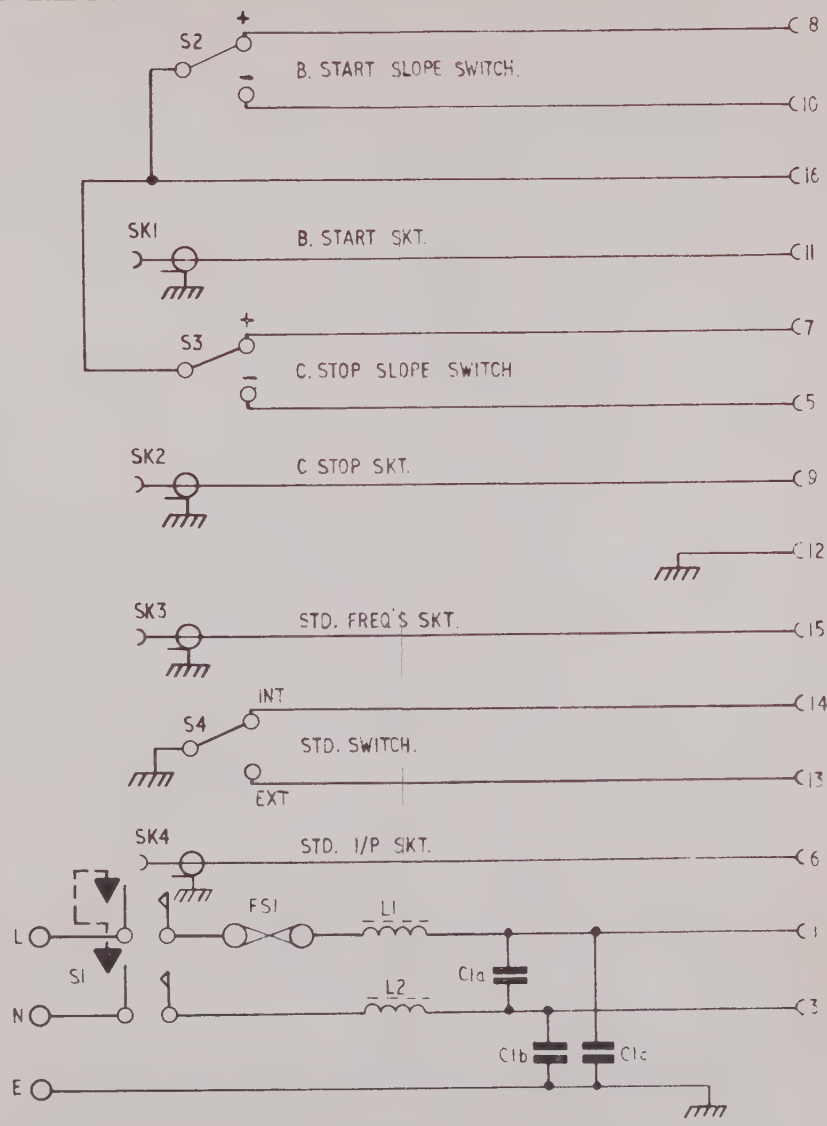
* OR CARD: TYPE 77/511 (OPTION K.)
TYPE 77/510 (OPTION L.)

NOTE: NOT TO SCALE.
NOT ALL COMPONENTS ARE SHOWN.

DIGITAL COUNTER MODEL 7737
LAYOUT DIAGRAM

S69/84

VENNER A DIV OF AMF. INT. LTD

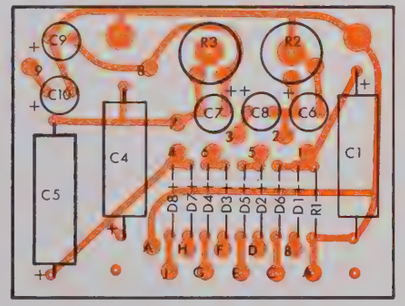


REAR PANEL
CIRCUIT DIAGRAM
TYPE 77/020
DRG No E68/93

COMPONENTS LIST — CL.77/220

POWER SUPPLY TYPE 77/220 (DRG. E68/92)

	Value or Type	Description	Venner Part No.
Capacitors			
C1	8µF (350V)	Electrolytic	X20643/50
C2	800µF (40V)	"	" /35
C3	2000µF (16V)	Aluminium foil	" /68
C4,5	250µF (40V)	" "	" /76
C6,7	100µF (3V)	Tantalum	Y50518/3
C(8-10)	15µF (16V)	"	" /4
Diodes			
D1,6	BYX10	-	X20639/35/P
D2,5,7,8	1N4002	-	" /60/P
D3,4	1N4001	-	" /45/P
Integrated Circuits			
X1	LO36T1	-	X50520/28
X2	LO05T1	-	" /29
X3	LO37T1	-	" /30
Resistors			
R1	470kΩ ±5% ¼W HS	Carbon	X5050/17/P
R2,3	220Ω ±20% ¼W	Carbon Lin.	X20999/82
Transformer			
T1	Mains transformer	-	Y51872



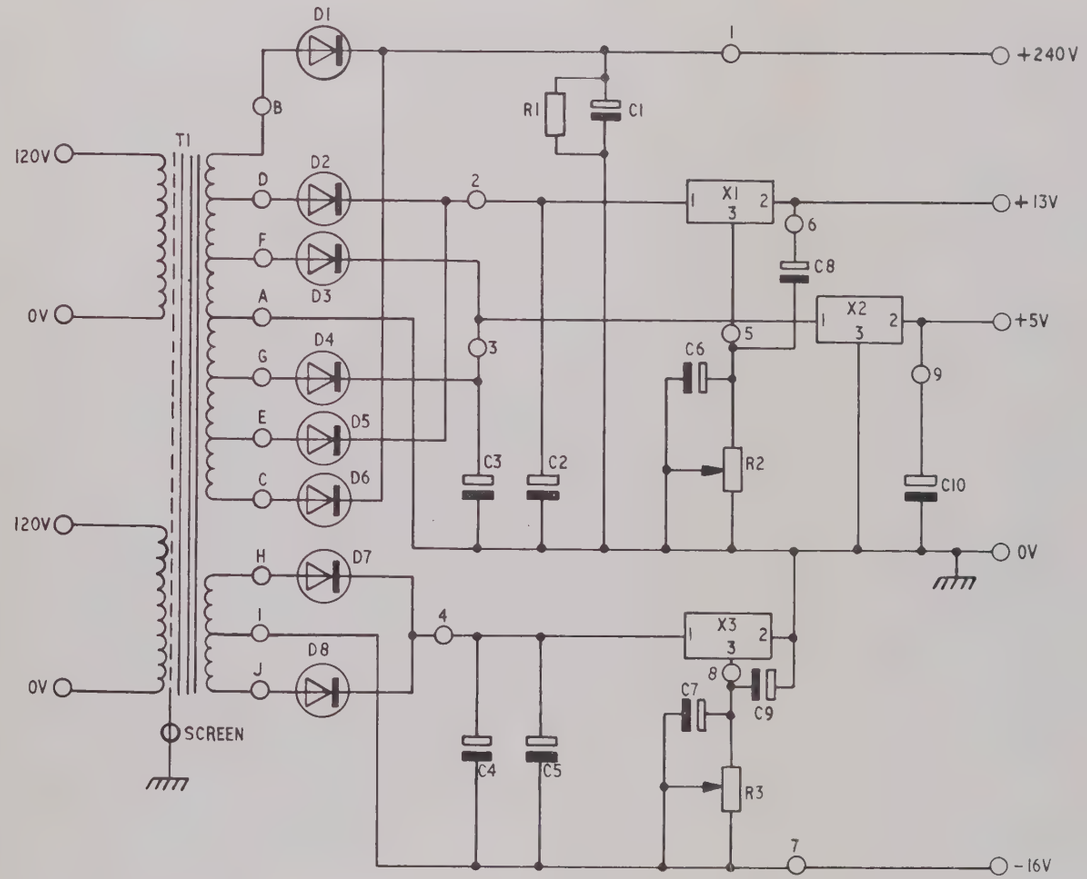
VIEWED FROM NON-COMPONENT SIDE.

SCALE 3/4 FULL SIZE.

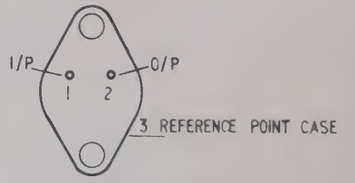
REF.
M2703

POWER SUPPLY
TYPE 77/220

BL
77/220



PIN CONNECTION	SECONDARY O/P
B	207V
D	18V
F	9·5V
A	0V
G	9·5V
E	18V
C	207V
H	22V
I	0V
J	22V



VIEWED FROM UNDERSIDE

POWER SUPPLY
CIRCUIT DIAGRAM
TYPE 77/220
DRG. NO. E68/92

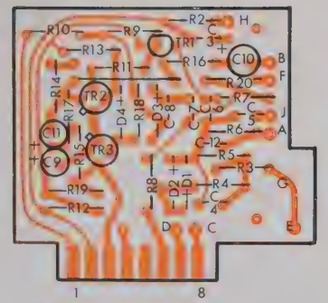
COMPONENTS LIST _____ CL.77/300

PRE-AMP TYPE 77/300 (DRG. E68/95)

	Value or Type	Description	Venner Part No.
Capacitors			
C1	0.1µF ±10% (400V)	Metalised Polyester	X23914/45
C2,11	3.3µF (16V)	Tantalum	X50518/1
C3,(6-8)	0.047µF +50% -25%	Polystyrene & Ceramic	X20641/55
C4	33pF ±10%	Ceramic	" /50
C5	1000pF ±20%	"	" /62
C9	33µF (10V)	Tantalum	Y50518/2
C10	100µF (3V)	"	" /3
C12	150pF ±10%	Ceramic	X20641/61
Diodes			
D1,2	BAW62	-	X20639/58
D3	BZY88/C7V5	-	" /42
D4	BZY88/C4V7	-	" /33
Resistors			
R1	500kΩ ±20% 0.2W	Carbon Lin.	*
R2	56kΩ ± 5% ⅛W	Carbon film	X50517/46
R3,21	10Ω " "	" "	" /1
R4,7,20	3.9MΩ ±10% "	" "	" /68
R5	1MΩ ± 5% "	" "	" /61
R6	220kΩ " "	" "	" /53
R8	470kΩ " "	" "	" /57
R9	2.2kΩ " "	" "	" /29
R10	680Ω " "	" "	" /23
R11	100Ω " "	" "	" /13
R12	150Ω " "	" "	" /15
R13,17	820Ω " "	" "	" /24
R14	220Ω " "	" "	" /17
R15	1.5kΩ " "	" "	" /27
R16	47Ω " "	" "	" /9
R18	18kΩ " "	" "	" /40
R19	470Ω " "	" "	" /21
Socket			
SK1	BNC	-	X50508/4
Switches			
S1	1p. ON/OFF	-	*
S2 (a-b)	2p. 3pos. toggle	-	X52057
Transistors			
TR1	2N5486	-	X20638/96
TR2,3	BFY90	-	" /95

*R1 ganged to switch S1: common part number X20999/83

Ref. P2241: 2/1C,2A



VIEWED FROM NON-COMPONENT SIDE.

VIEWED FROM COMPONENT SIDE.

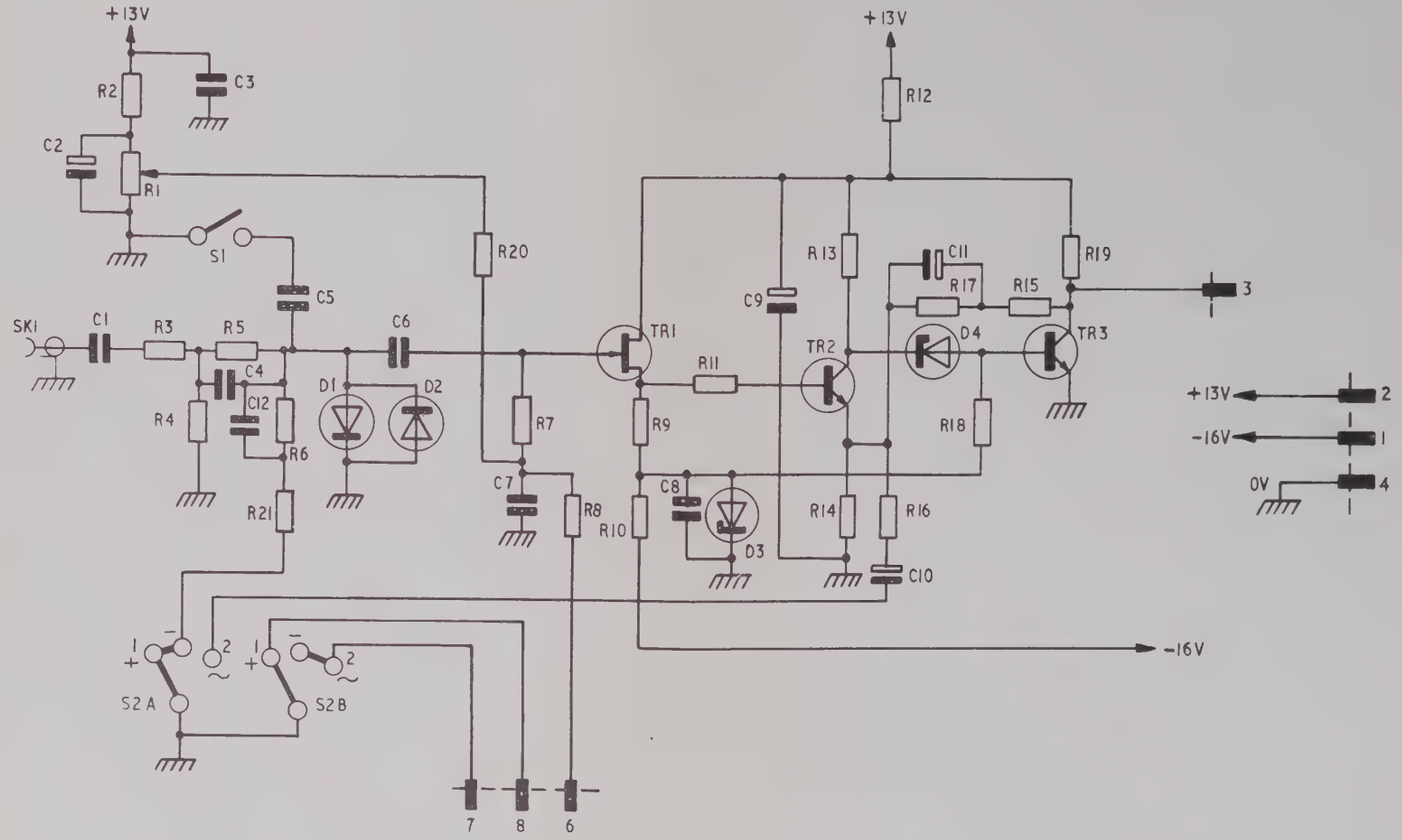
SCALE 3/4 FULL SIZE.

REF.
M2615
M2658

PRE-AMP.

TYPE 77/300

BL
77/300



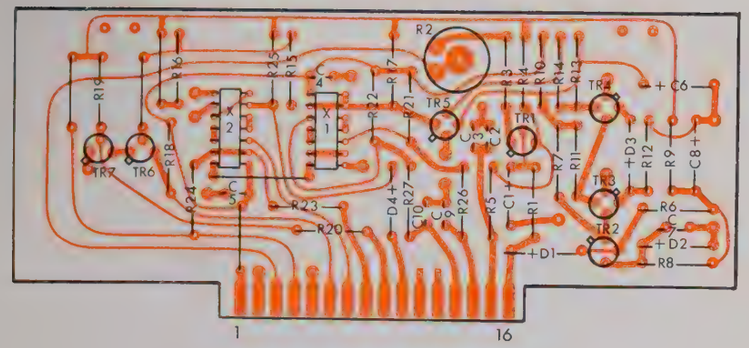
NOTE: CONNECTIONS THUS: —— REFER TO EDGE CONNECTOR.

PRE AMP
CIRCUIT DIAGRAM
TYPE 77/300
DRG. NO. E68/95

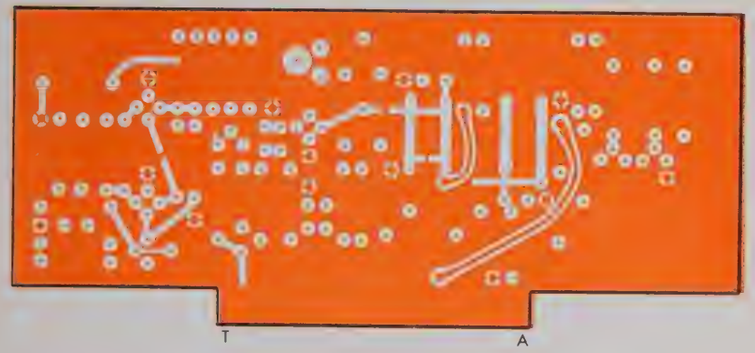
COMPONENTS LIST — CL.77/310

PULSE SHAPER TYPE 77/310 (DRG. E68/94)

	Value or Type	Description	Venner Part No.
Capacitors			
C1	2.2uF (20V)	Tantalum	Y22776/22
C(2-5),7,9,10	0.047uF + 5% -25%	Polystyrene & Ceramic	X20641/55
C6	33uF (10V)	Tantalum	Y22776/16
C8	15uF (20V)	"	" /20
Diodes			
D1	BZY88/C4V7	-	X20639/33
D2	U2973	-	" /31
D3	BAW62	-	" /58
D4	OA202	-	" /48
Integrated Circuits			
X1,2	SN7300N	-	X50520/25
Resistors			
R1	9.1kΩ ± 5% ¼W HS	Carbon	X50500/72/P
R2	1kΩ ±20%	Carbon Lin.	X20999/58
R3,20,23	1.5kΩ ± 5% ¼W HS	Carbon	X50500/53/P
R4	4.3kΩ " " "	"	" /64/P
R5	1MΩ " " "	"	X50501/25/P
R6	15kΩ " " "	"	X50500/77/P
R7,17	1kΩ " " "	"	" /49/P
R8	1.8kΩ " " "	"	" /55/P
R9	220Ω " " "	"	" /33/P
R10,12	10Ω " " "	"	" /1/P
R11	430Ω " " "	"	" /40/P
R13	200Ω " " "	"	" /32/P
R14	100Ω " " "	"	" /25/P
R15,21,22	2.2kΩ " " "	"	" /57/P
R16	22kΩ " " "	"	" /81/P
R18	750Ω " " "	"	" /46/P
R19	33kΩ " " "	"	" /85/P
R24	3.6kΩ " " "	"	" /62/P
R25	4.7kΩ " " "	"	" /65/P
R26,27	47Ω " " "	"	" /17/P
Transistors			
TR1,2	V405A	-	X20638/65
TR(3-5)	BFY90	-	" /95
TR6,7	U15718/2	-	" /55



VIEWED FROM NON-COMPONENT SIDE.



VIEWED FROM COMPONENT SIDE.

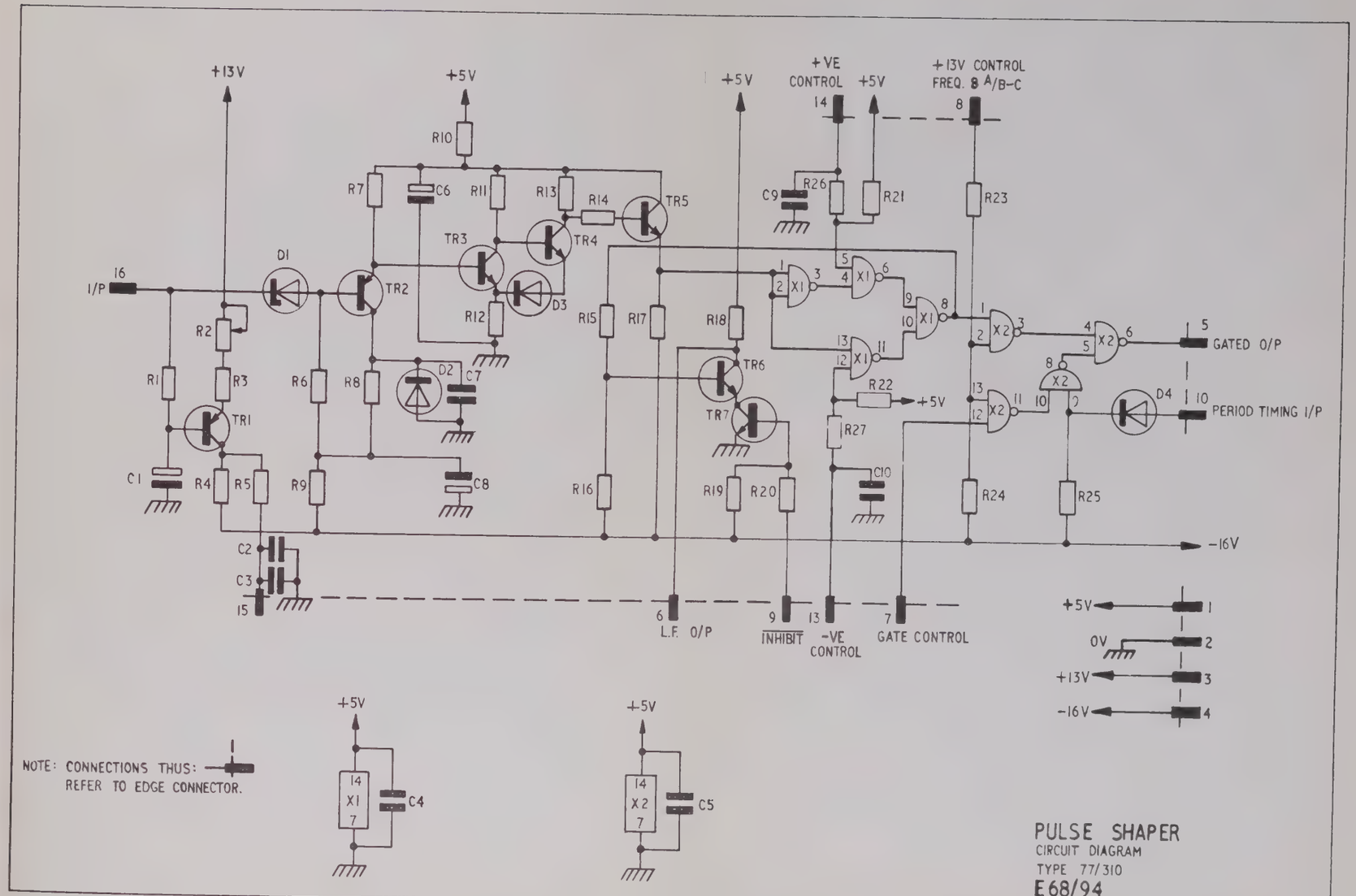
SCALE 3/4 FULL SIZE.

REF.
M2659
M2660

PULSE SHAPER

TYPE 77/310

BL 77/310



PULSE SHAPER
CIRCUIT DIAGRAM
TYPE 77/310
E68/94

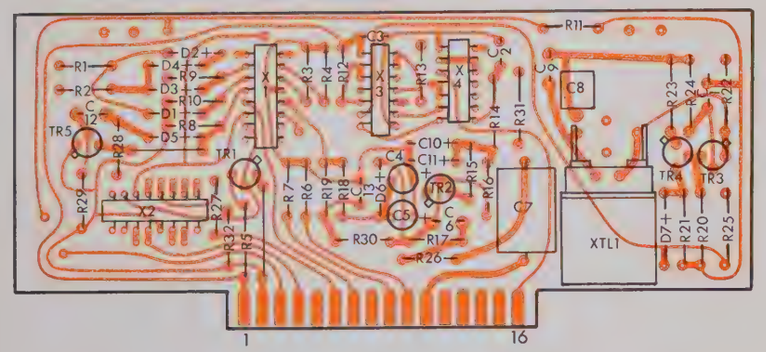
OSCILLATOR AND DIVIDER TYPE 77/500 (DRG. E69/02)

	Value or Type	Description	Venner Part No.
Capacitors			
C1,2,3,13	0.047uF +50% -25%	Polystyrene & Ceramic	X20641/55
C4,5	33uF (10V)	Tantalum	Y50518/2
C6	22pF ±10%	Ceramic	Y50509/2
C7	0.22uF ±10% (250V)	Metallised film	X23914/51
C8	2-18pF (Trimmer)	Air spaced	Z21135/11
C9*	10pF ± 5%	Ceramic	Y50509/1
C10,11	6.8uF (6V)	Elect. Tantalum	Y22776/23
C12	56pF ± 5%	Ceramic	Y50509/5
Crystal			
XTL1	10MHz	Glass style L	X20650/17
Diodes			
D(1-5)	U2973/2	-	X20639/31
D6	IN4009	-	" /41
D7	BZY88/C6V2	-	" /37/P
Integrated Circuits			
X1,2	C16	-	X50520/24
X3	SN7413N	-	" /21
X4	SN7400N	-	" /1
Resistors			
R1,2,15,18	3.3kΩ ±5% ⅛W	Carbon film	X50517/31
R3,4,6,7,19,28	10kΩ " "	" "	" /37
R5	1kΩ ±5% ¼W HS	Carbon	X50500/49/P
R(8-10)	100kΩ " ⅛W	Carbon film	X50517/48
R11	10Ω " "	" "	" /1
R12,13	8.2kΩ " "	" "	" /36
R14	47Ω " ¼W HS	Carbon	X50500/17/P
R16	18kΩ " ⅛W	Carbon film	X50517/40
R17	22kΩ " "	" "	" /41
R20	2.4kΩ " ¼W HS	Carbon	X50500/58/P
R21	560Ω " " "	"	" /43/P
R22	3.6kΩ " " "	"	" /62/P
R23	180Ω " " "	"	" /31/P
R24	75Ω " " "	"	" /22/P
R25	7.5kΩ " " "	"	" /70/P
R26	470Ω " ⅛W	Carbon film	X50517/21
R27,29,32	3.9kΩ " "	" "	" /32
R30	12kΩ ±5% ⅛W	" "	" /38
R31	330Ω " ¼W HS	Carbon	X50500/37/P

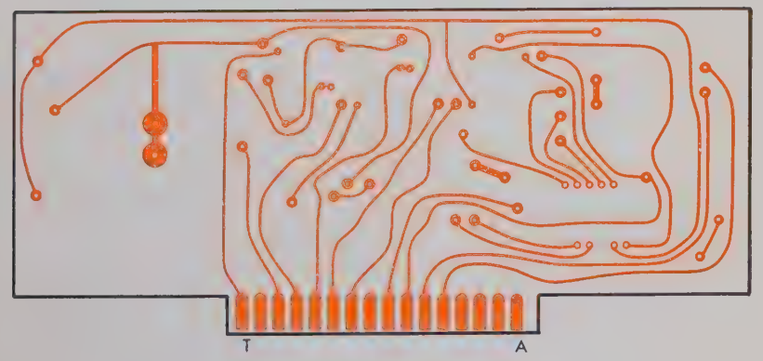
* For crystals (XTL1) colour coded with a red mark the value of C9 is 100pF or 120pF as determined on test.

	Value or Type	Description	Venner Part No.
Transistors			
TR1,2,3,4,5	U1518/2	-	X20638/55
TR2*	BC108	-	" /71

* Gain not less than 71



VIEWED FROM NON-COMPONENT SIDE.



VIEWED FROM COMPONENT SIDE.

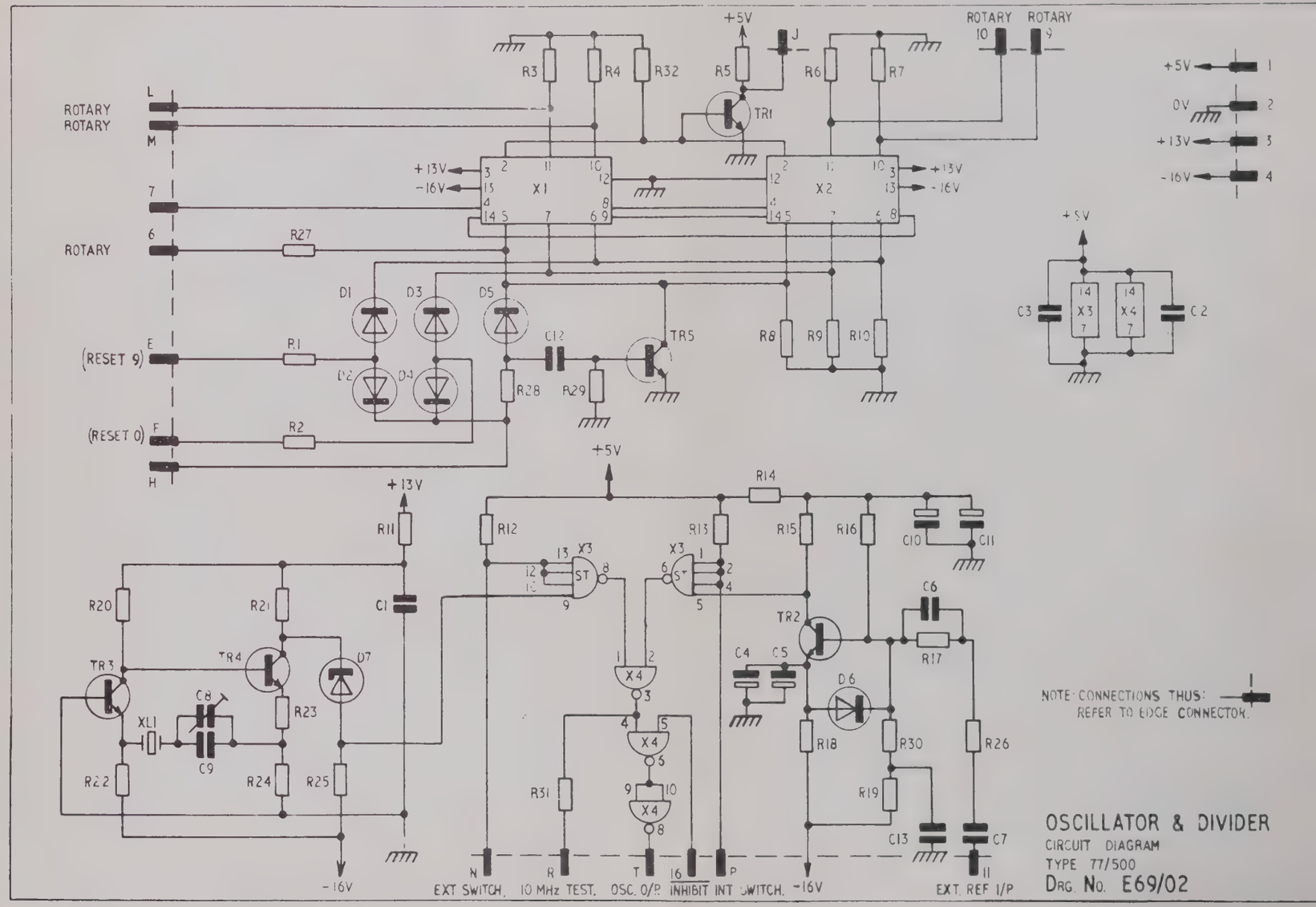
SCALE 3/4 FULL SIZE.

REF.
M2672
M2673

OSCILLATOR & DIVIDER

TYPE 77/500

BL 77/500



OSCILLATOR & DIVIDER

CIRCUIT DIAGRAM

TYPE 77/500

DRG. NO. E69/02

COMPONENTS LIST — CL.77/510 & 511

Sheet 1

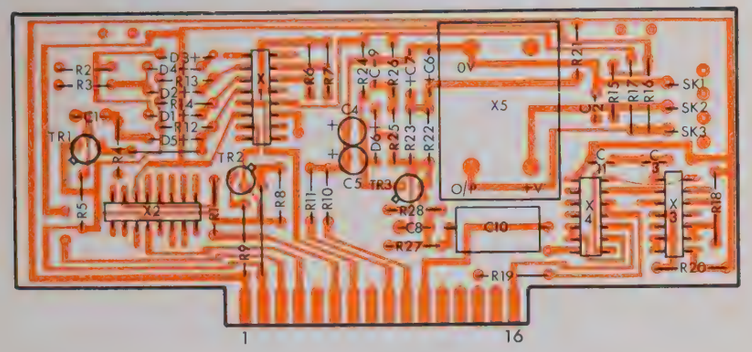
OSCILLATOR AND DIVIDER TYPES 77/510 AND 77/511 (DRG. E69/22)

NOTE Components and values are applicable to both types of card except where otherwise marked.

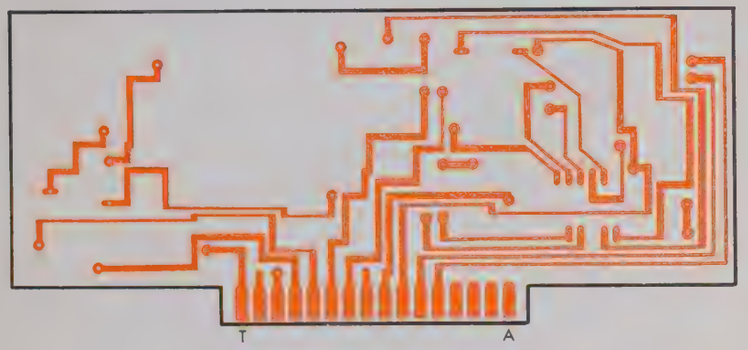
	Value or Type	Description	Venner Part No.
Capacitors			
C1	56pF ± 5%	Ceramic	Y50509/5
C2,3,9,11	0.047uF +50%	Polystyrene &	
	-25%	Ceramic	X20641/55
C4,5	33uF (10V)	Tantalum	Y50518/2
C6,7	6.8uF (6V)	Elect. Tantalum	X22776/23
C8	22pF ±10%	Ceramic	Y50509/2
C10	0.22uF ±10% (250V)	Metallised film	X23914/51
Diodes			
D(1-5)	U2973/2	-	X20639/31
D6	IN4009	-	" /41
Integrated Circuits			
X1,2	C16	-	X50520/24
X3	SN7413N	-	" /21
X4	SN7400N	-	" /1
Oscillators			
X5 Card type 77/510:	3181-01	10MHz	Z51276
" " 77/511:	QC1223	10MHz	Y52146
Plugs(Card type 77/510 only)			
PL1	Black	-	X50508/34
PL2	Red	-	" /35
PL3	Green	-	" /36
Resistors			
R1,5,8	3.9kΩ ±5% ⅛W	Carbon film	X50517/32
R2,3,22,24	3.3kΩ " "	" "	" /31
R4,6,7,10,11,26	10kΩ " "	" "	" /37
R9	1kΩ " ¼W HS	Carbon	X50500/49/P
R(12-14)	100kΩ " ⅛W	Carbon film	X50517/48
R15 Card type 77/510:			
	22Ω " ⅛W	Carbon film	X50517/5
Card type 77/511:			
	1.5kΩ " "	Carbon film	" /27
R16	4.3kΩ " ¼W HS	Carbon	X50500/64/P
R17	4.7kΩ " " "	"	" /65/P
R18,20	8.2kΩ " " "	"	" /71/P
R19	330Ω " " "	"	" /37/P
R21	47Ω " ⅛W	Carbon film	X50517/9
R23	18kΩ " "	" "	" /40
R25	12kΩ " "	" "	" /38

	Value or Type	Description	Venner Part No.
R27	470Ω ±5% ⅛W	Carbon film	X50517/21
R28	22kΩ " "	" "	" /41
Sockets (Card type 77/510 only)			
SK(1-3)	50S/PCB	-	X50508/33
Transistors			
TR1,2	U1518/2	-	X20638/55
TR3	BC108	-	" /71

Ref: P2266: 2/1-2-
P2267: 1/1-



VIEWED FROM NON-COMPONENT SIDE.



VIEWED FROM COMPONENT SIDE.

SCALE 3/4 FULL SIZE.

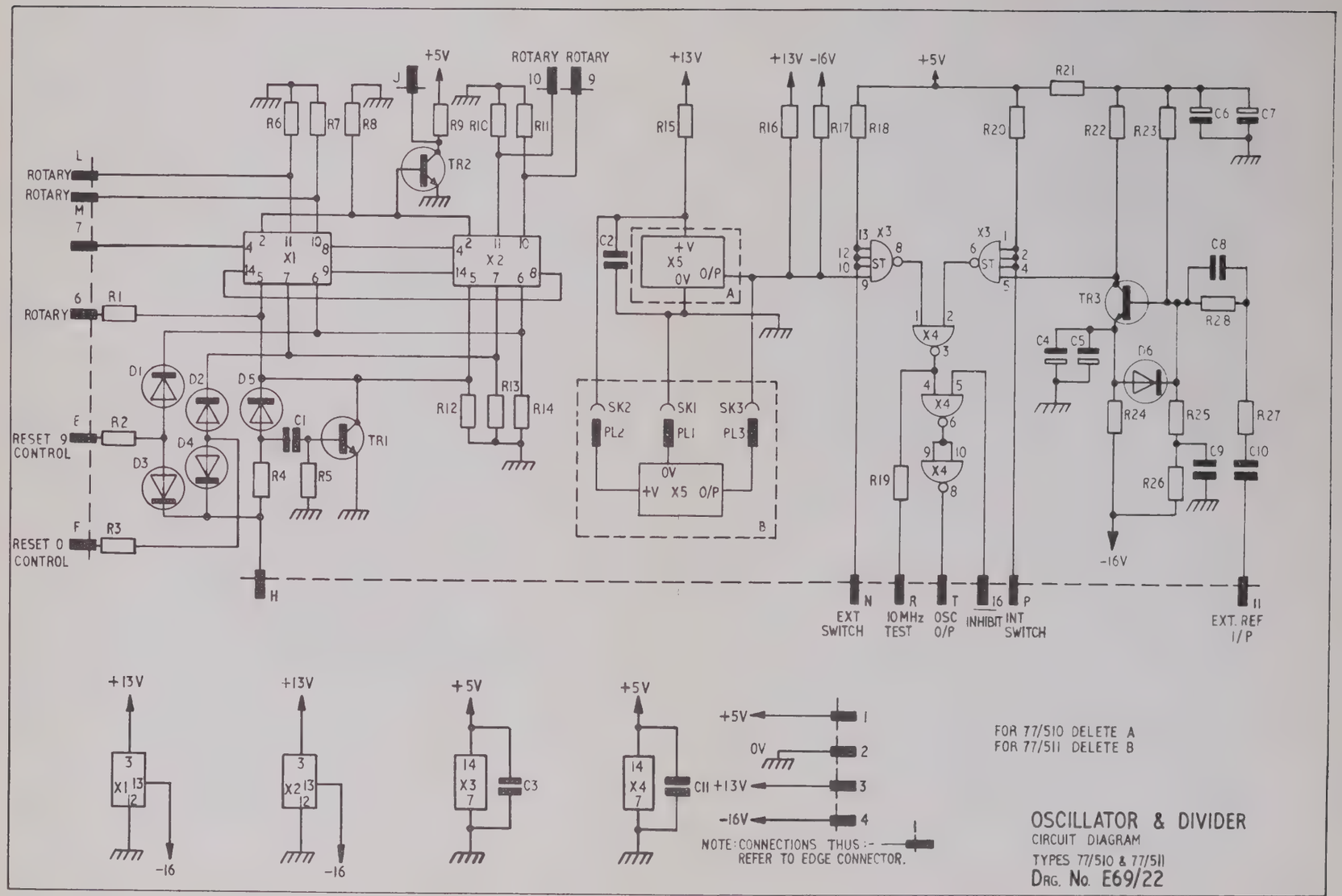
NOTE. FOR TYPE 77/510 X5 IS MOUNTED REMOTELY.

REF.
M2771
M2770

OSCILLATOR & DIVIDER

TYPES 77/510 & 77/511

BL
77/510
& 77/511



OSCILLATOR & DIVIDER

CIRCUIT DIAGRAM

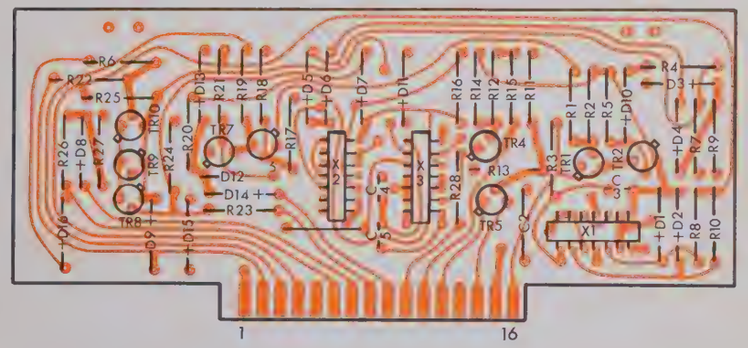
TYPES 77/510 & 77/511

DRG. No. E69/22

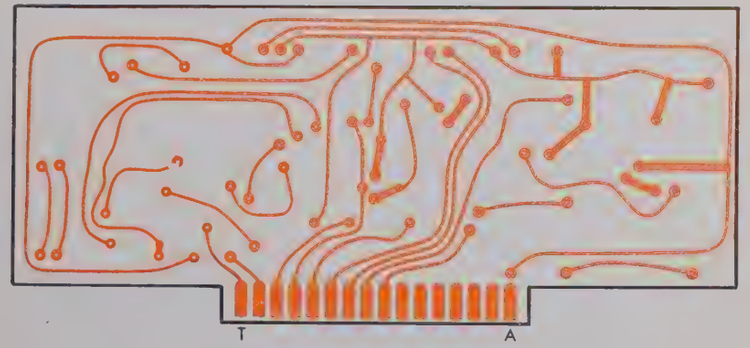
COMPONENTS LIST CL.77/400

DIVIDER INTERFACE TYPE 77/400 (DRG. E68/100)

	Value or Type	Description	Venner Part No.
Capacitors			
C2	0.0047µF ±10% (250V)	Metallised film	X23914/40
C3,4,5	0.047µF +50% -25%	Polystyrene & Ceramic	X20641/55
Diodes			
D(1-16)	U2973/2	-	X20639/31
Integrated Circuits			
X1,3	SN7400N	-	X50520/1
X2	SN7900N	-	" /5
Resistors			
R1,17	2.4kΩ ±5% ¼W HS	Carbon	X50500/58/P
R2,3,5,18	430Ω " " "	"	" /40/P
R4,25	2.2kΩ " " "	"	" /57/P
R6	2.7kΩ " " "	"	" /59/P
R7,9,15,20	3.3kΩ " " "	"	" /61/P
R8,10	9.1kΩ " " "	"	" /72/P
R11	8.2kΩ " " "	"	" /71/P
R12	7.5kΩ " " "	"	" /70/P
R13,16	1kΩ " " "	"	" /49/P
R14,22	3.9kΩ " " "	"	" /63/P
R19	1.5kΩ " " "	"	" /53/P
R21	15kΩ " " "	"	" /77/P
R23,26	4.7kΩ " " "	"	" /65/P
R24,27	10kΩ " " "	"	" /73/P
R28	820Ω " " "	"	" /47/P
Transistors			
TR1,2,(4-9)	U1518/2	-	X20638/55
TR10	V405A	-	" /65



VIEWED FROM NON-COMPONENT SIDE



VIEWED FROM COMPONENT SIDE.

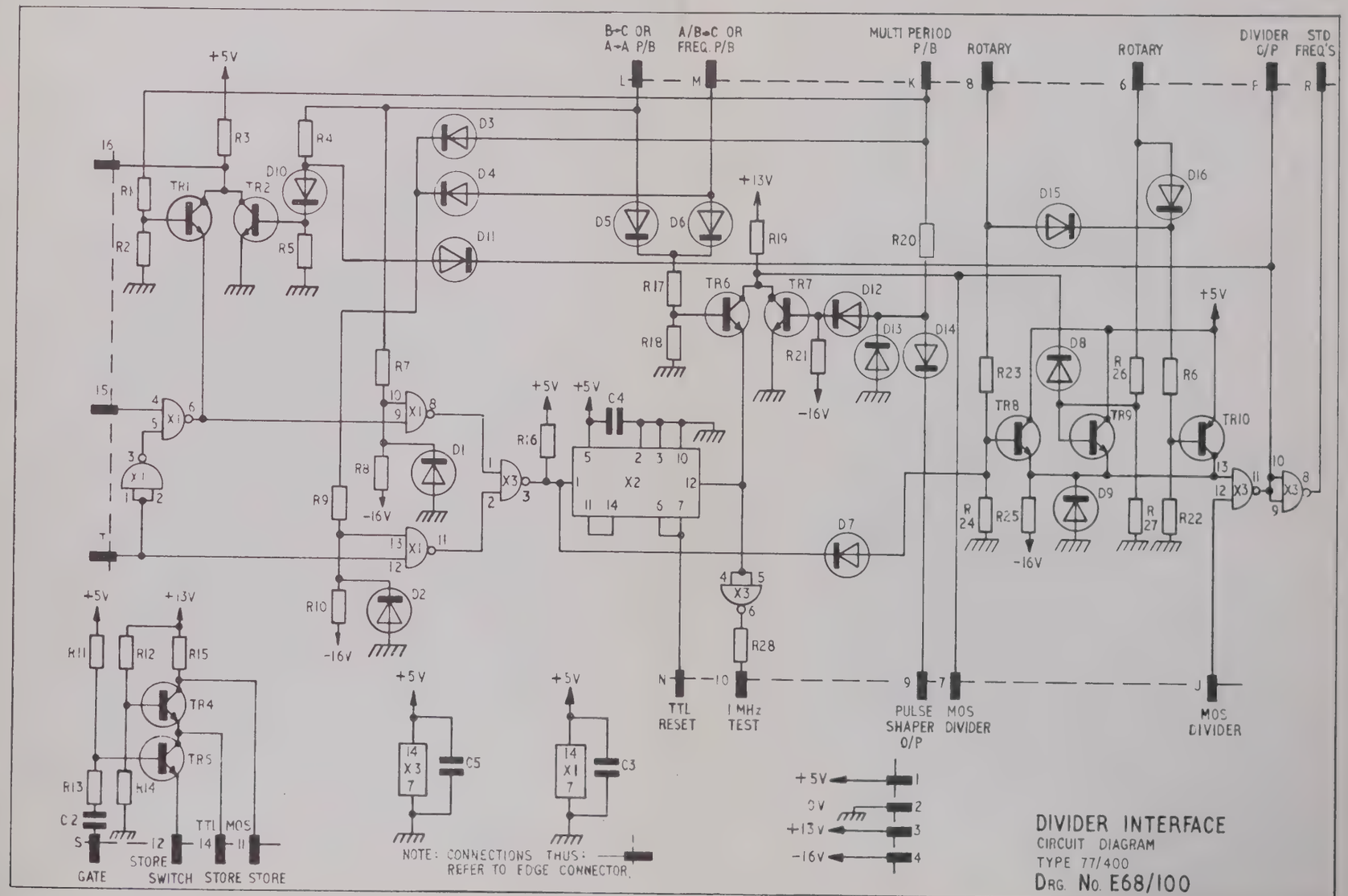
SCALE 3/4 FULL SIZE.

REF.
M2674
M2675

DIVIDER INTERFACE

TYPE 77/400

BL 77/400



DIVIDER INTERFACE
CIRCUIT DIAGRAM
TYPE 77/400
DRG. NO. E68/100

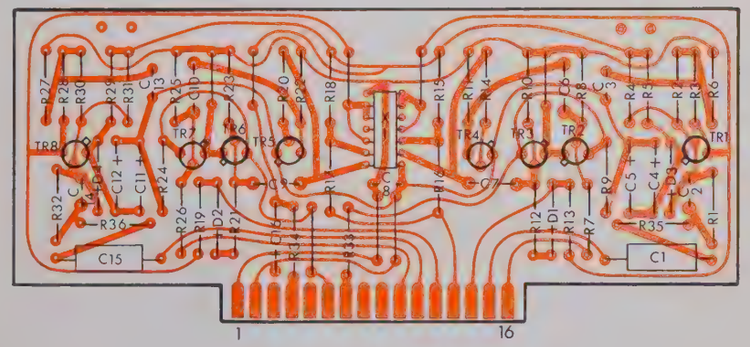
COMPONENTS LIST CL.77/320

STOP AND START SHAPERS TYPE 77/320 (DRG. E69/01)

	Value or Type	Description	Venner Part No.
Capacitors			
C1,15	0.22µF ±10% (250V)	Metallised film	X23914/51
C2,14	47pF ± 5%	Ceramic	Y50509/4
C3,8,13	0.047µF +50% -25%	Polystyrene & Ceramic	X20641/55
C4,5,11,12	47µF (6V)	Tantalum	Y22776/14
C6,7,9,10	100pF ± 5%	Ceramic	Y50509/7
C16	15µF (20V)	Tantalum	Y22776/20
Diodes			
D1,2	1N4009	-	X20639/41/P
D3,4	U2973/2	-	" /31/P
Integrated Circuit			
X1	SN7413N	-	X50520/21
Resistors			
R1,32	20kΩ ±5% ¼W HS	Carbon	X50500/80/P
R2,30	18kΩ " " "	"	" /79/P
R3,5,16,17,28,29	3.3kΩ " " "	"	" /61/P
R4,31	22kΩ " " "	"	" /81/P
R6,27,34	47Ω " " "	"	" /17/P
R7,26	510Ω " " "	"	" /42/P
R(8-11),(22-25)	560Ω " " "	"	" /43/P
R12,21,35,36	470Ω " " "	"	" /41/P
R13,19	5.1kΩ " " "	"	" /66/P
R14,20	1kΩ " " "	"	" /49/P
R15,18	9.1kΩ " " "	"	" /72/P
R33	100Ω " " "	"	" /25/P
Transistors			
TR1*,8*	BC108	-	X20638/71
TR2,3,6,7	V405A	-	" /65
TR4,5	U1518/2	-	" /55

* Gain not less than 71

Ref: P2247: 1/1A



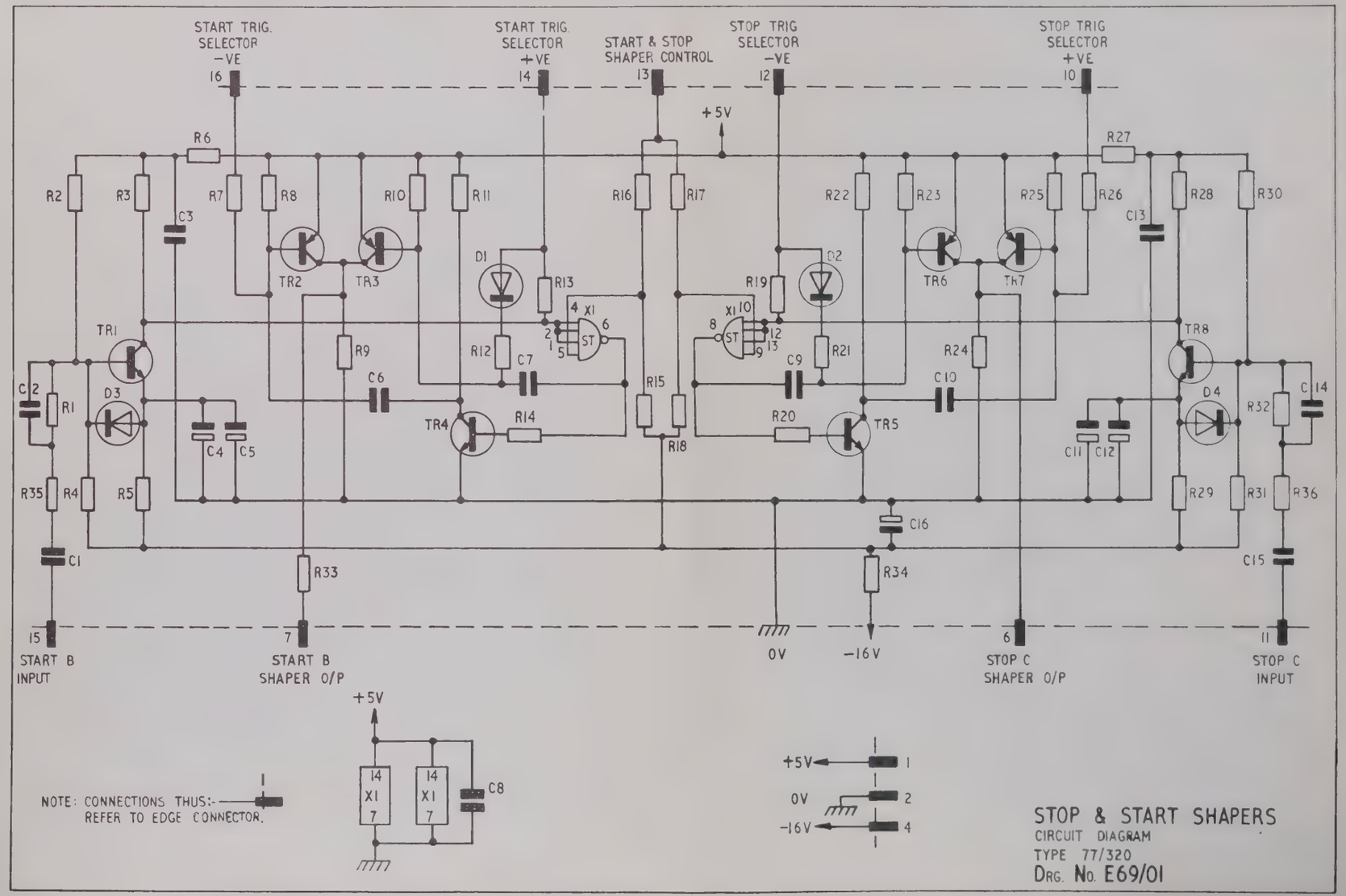
VIEWED FROM NON-COMPONENT SIDE.

SCALE 3/4 FULL SIZE.

REF.
M2663

STOP & START SHAPERS
TYPE 77/320

BL
77/320



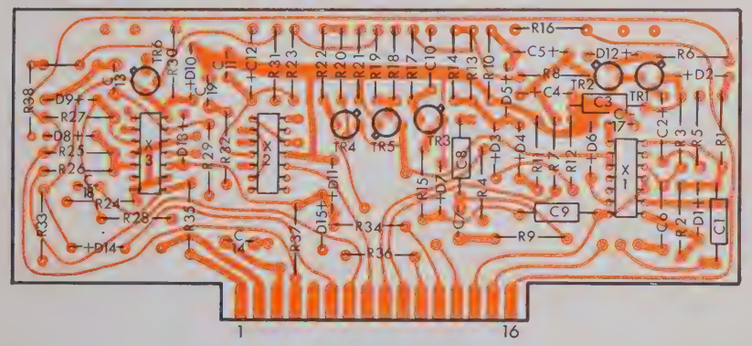
STOP & START SHAPERS
CIRCUIT DIAGRAM
TYPE 77/320
DRG. NO. E69/01

GATE CONTROL AND RESET TYPE 77/600 (DRG.E68/99)

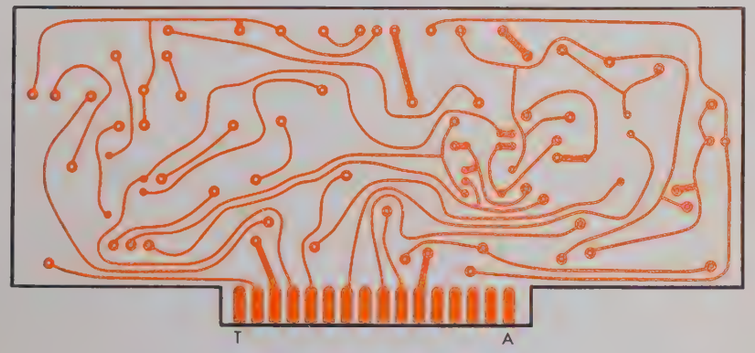
	Value or Type	Description	Venner Part No.
Capacitors			
C1,3	0.047µF ±10% (250V)	Metallised film	X23914/38
C2	15µF (20V)	Tantalum	Y22776/20
C5	2.2µF (20V)	Tantalum	Y22776/22
C6,10	0.0047µF ±10% (250V)	Metallised film	X23914/40
C7*	10pF ± 5%	Ceramic	Y50509/1
C8*,9	0.1µF ±10% (250V)	Metallised film	X23914/27
C11,17,18	0.047µF +50% -25%	Polystyrene & Ceramic	X20641/55
C12	33µF (10V)	Tantalum	Y22776/16
C13,14	1000pF ±10%	Ceramic	Y50509/11
C19	47pF ± 5%	"	" /4
Diodes			
D1,2,3*,4,5,(8-15)	U2973/2	-	X20639/31
D6,7	IN4009	-	" /41
Integrated Circuits			
X1	SN7400N	-	X50520/1
X2	SN7473N	-	" /18
X3	SN7401N	-	" /26
Resistors			
R1	3.9kΩ ±5% ¼W HS	Carbon	X50500/63/P
R2	5.6kΩ " " "	"	" /67/P
R3,16	4.7kΩ " " "	"	" /65/P
R4,10,11,12*,13*,17	10kΩ " " "	"	" /73/P
R5	47Ω " " "	"	" /17/P
R6,25,27,37	9.1kΩ " " "	"	" /72/P
R7	12Ω " " "	"	" /3/P
R8	47kΩ " " "	"	" /89/P
R9*,18,34,36,31	1kΩ " " "	"	" /49/P
R14	5.1kΩ " " "	"	" /66/P
R15	22kΩ " " "	"	" /81/P
R19	8.2kΩ " " "	"	" /71/P
R20	7.5kΩ " " "	"	" /70/P
R21,30	6.8kΩ " " "	"	" /69/P
R22,26,28,38	3.3kΩ " " "	"	" /61/P
R23,35	10Ω " " "	"	" /1/P
R24	470Ω " " "	"	" /41/P
R29,32	100Ω " " "	"	" /25/P
R33	2.2kΩ " " "	"	" /57/P

* Fitted only for Ext. Reset Input facility

	Value or Type	Description	Venner Part No.
Transistors			
TR1	V435	-	X20638/72
TR2,3	BC108	-	" /71
TR4,5	U1518/2	-	" /55
TR6	V4054	-	" /65



VIEWED FROM NON-COMPONENT SIDE.



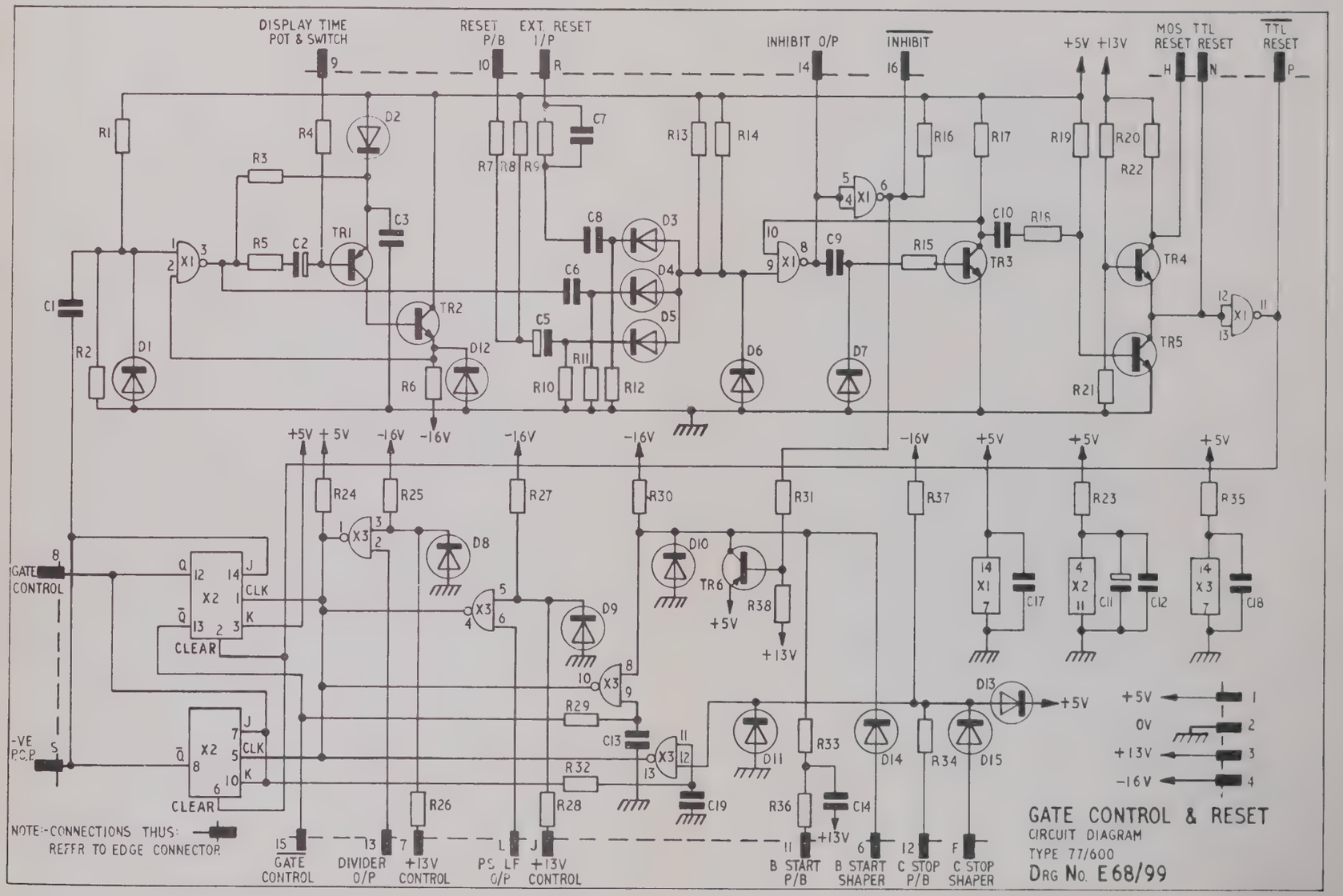
VIEWED FROM COMPONENT SIDE.

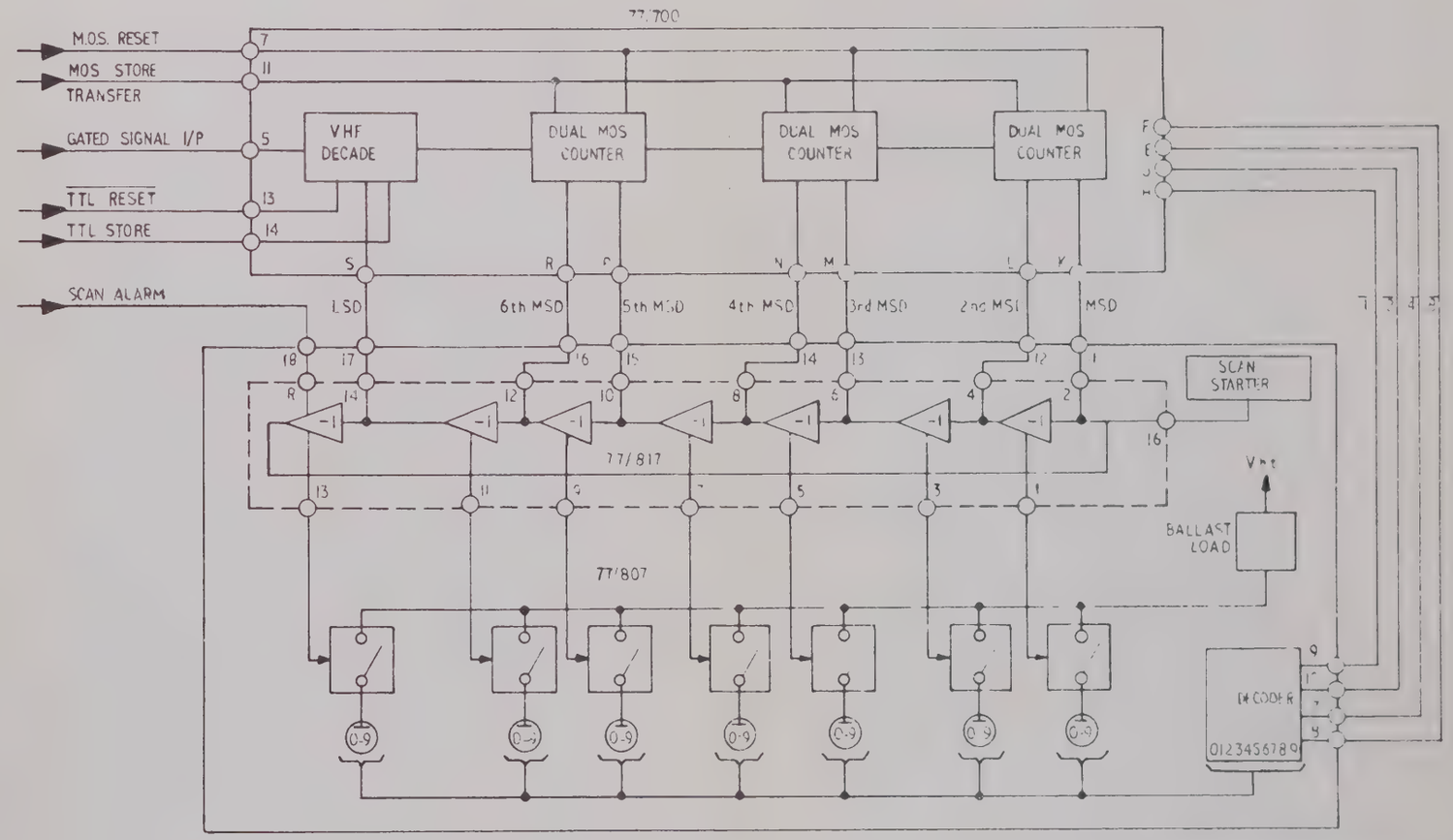
SCALE 3/4 FULL SIZE.

REF.
M2670
M2671

GATE CONTROL & RESET
TYPE 77/600

BL
77/600



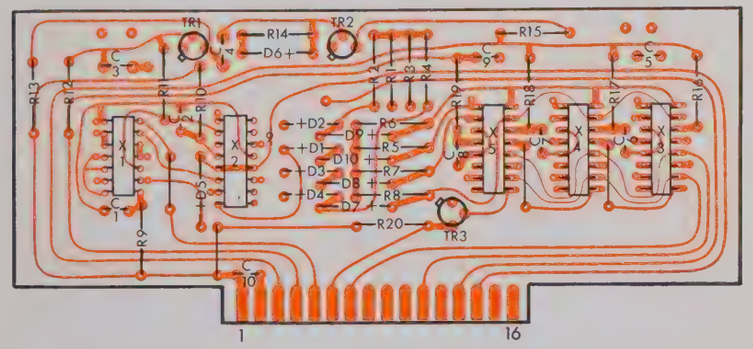


COUNTER & SCANNING DISPLAY
SCHEMATIC DIAGRAM
TYPE 77/700, 77/807 & 77/817
DRG NO E69/24

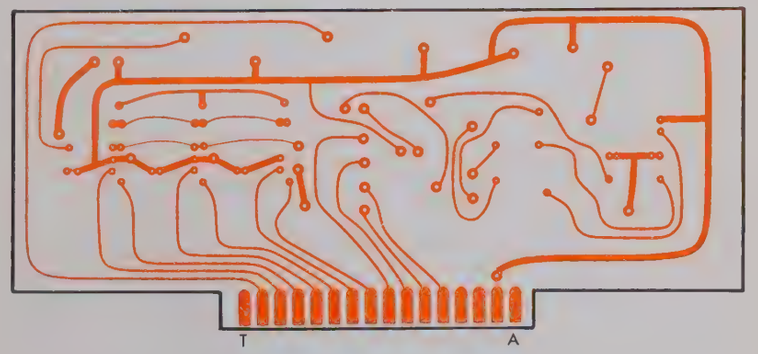
COMPONENTS LIST CL.77/700

COUNTER TYPE 77/700 (DRG. E68/98)

	Value or Type	Description	Venner Part No.
Capacitors			
C1,2,(5-10)	0.047µF +50% -25%	Polystyrene & Ceramic	X20641/55
C3	22pF ±10%	Ceramic	Y50509/2
C4	56pF ± 5%	"	" /5
Diodes			
D(1-4)	U2973/2	-	X20639/31
D(5-10)	"	-	" /31/P
Integrated Circuits			
X1	SN74196N (with red spot)	-	X50520/22
X2	SN7475N	-	" /23
X3	C16 (with red spot)	-	" /36
X4,5	C16	-	" /24
Resistors			
R(1-4)	12kΩ ±5% ¼W HS	Carbon	X50500/75/P
R(5-8)	2.7kΩ " " "	"	" /59/P
R9,10,(16-19)	10Ω " " "	"	" /1/P
R11,15	1kΩ " " "	"	" /49/P
R12	22kΩ " " "	"	" /81/P
R13	470Ω " " "	"	" /41/P
R14	680Ω " " "	"	" /45/P
Transistors			
TR1,2	U1518/2	-	X20638/55



VIEWED FROM NON-COMPONENT SIDE.



VIEWED FROM COMPONENT SIDE.

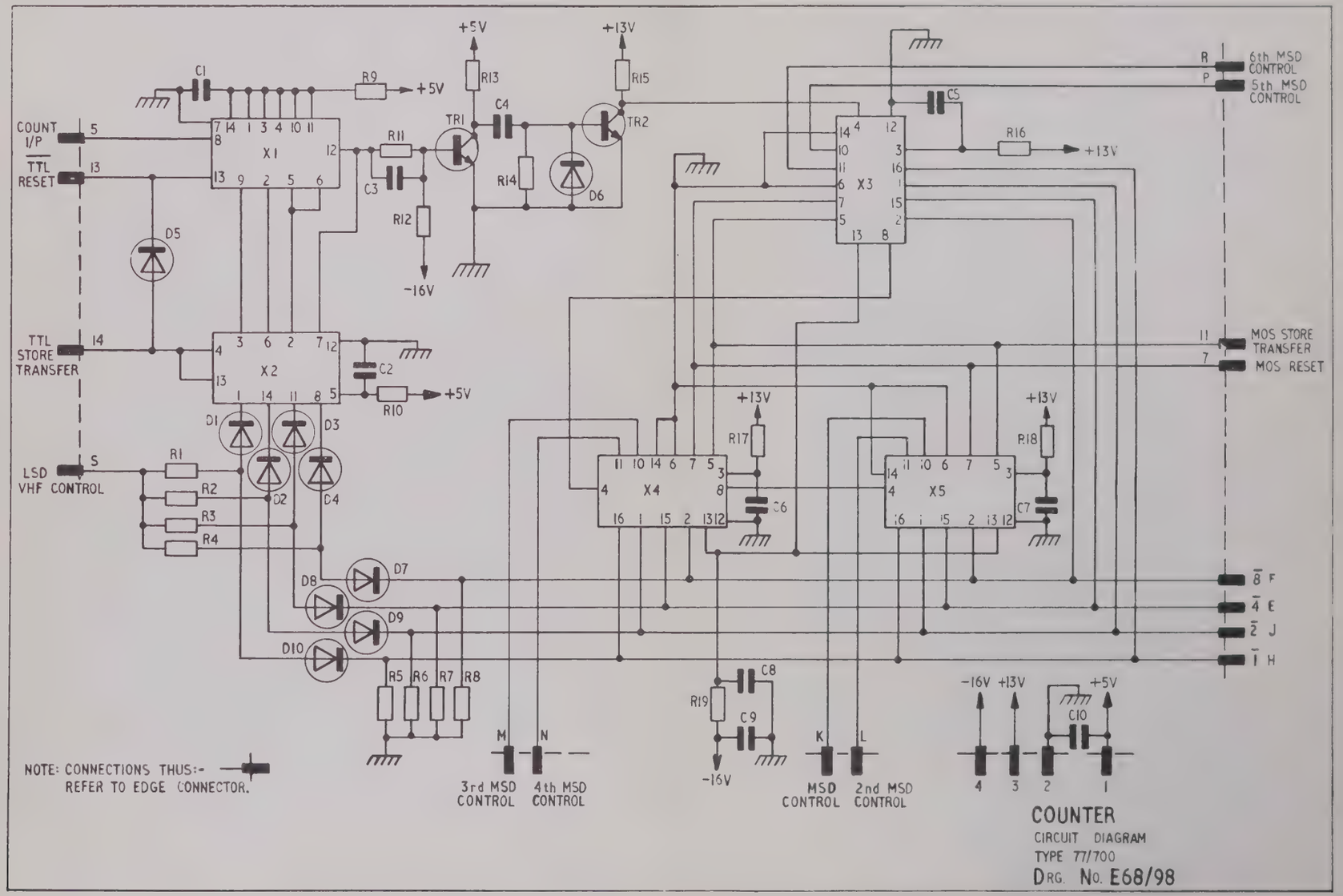
SCALE 3/4 FULL SIZE.

REF.
M2676
M2677

COUNTER

TYPE 77/700

BL
77/700

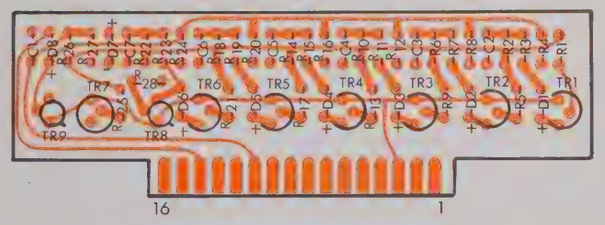


COUNTER
CIRCUIT DIAGRAM
TYPE 77/700
DRG. No. E68/98

COMPONENTS LIST CL.77/817

DISPLAY CONTROL TYPE 77/817 (DRG. E68/97)

	Value or Type	Description	Venner Part No.
Capacitors			
C(1-7)	0.047µF +50% -25%	Polystyrene & Ceramic	X20641/55
Diodes			
D(1-7)	BXY10	-	X20639/35
D8	U2973/2	-	" /31
Resistors			
R1,5,9,13,17, 21,25	12kΩ ±5% ¼W HS	Carbon	X50500/75
R2,6,10,14,18, 22	430Ω " " "	"	" /40
R3,7,11,15,19, 23	680Ω " " "	"	" /45
R4,8,12,16,20, 24,28	180kΩ " " "	"	X50501/7
R26	1kΩ " " "	"	X50500/49
R27	750Ω " " "	"	" 46
Transistors			
TR(1-7)	C407	-	X20638/69
TR8,9	BC108	-	" /71



VIEWED FROM NON-COMPONENT SIDE.

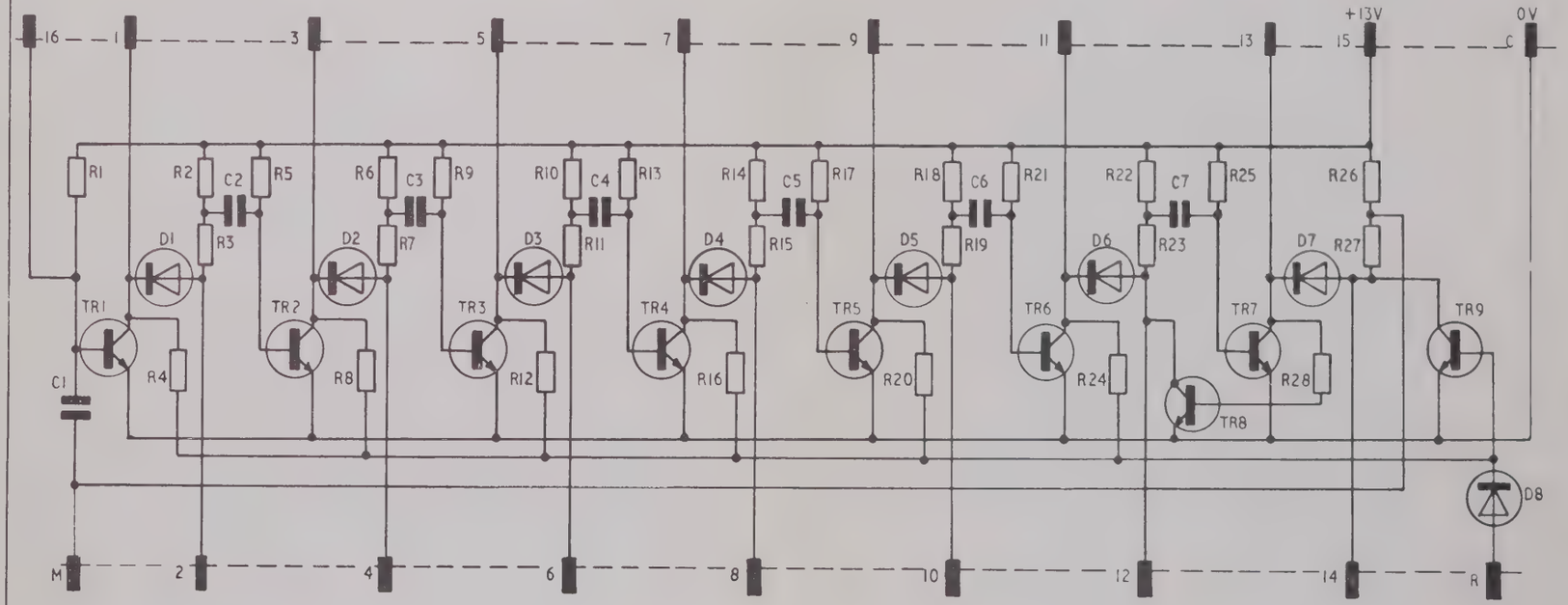
VIEWED FROM COMPONENT SIDE.

SCALE ¾ FULL SIZE.

REF.
M2666
M2667

DISPLAY CONTROL
TYPE 77/817

BL 77/817



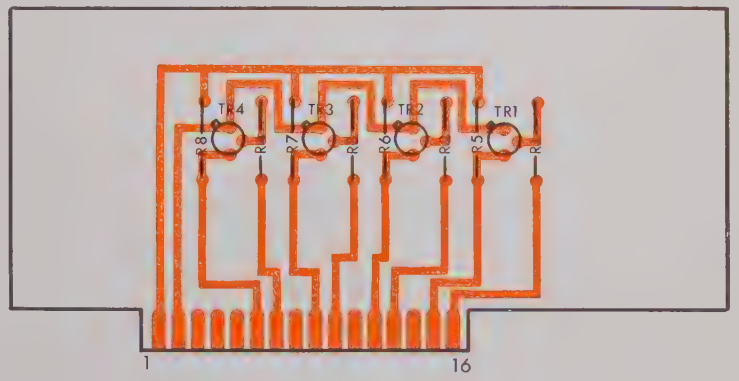
NOTE: CONNECTIONS THUS: —|— REFER TO EDGE CONNECTOR

DISPLAY CONTROL
CIRCUIT DIAGRAM
TYPE 77/817
DRG. NO. E68/97

COMPONENTS LIST _____ CL.77/910

SERIAL B.C.D. INTERFACE TYPE 77/910 (DRG. E69/33)

	Value or Type	Description	Venner Part No.
Resistors			
R(1-4)	8.2kΩ ±5% ¼W H.S.	Carbon	X50500/71/P
R(5-8)	27kΩ " " "	"	" /83/P
Transistors			
TR(1-4)	BC108	-	X20638/71



VIEWED FROM NON-COMPONENT SIDE.

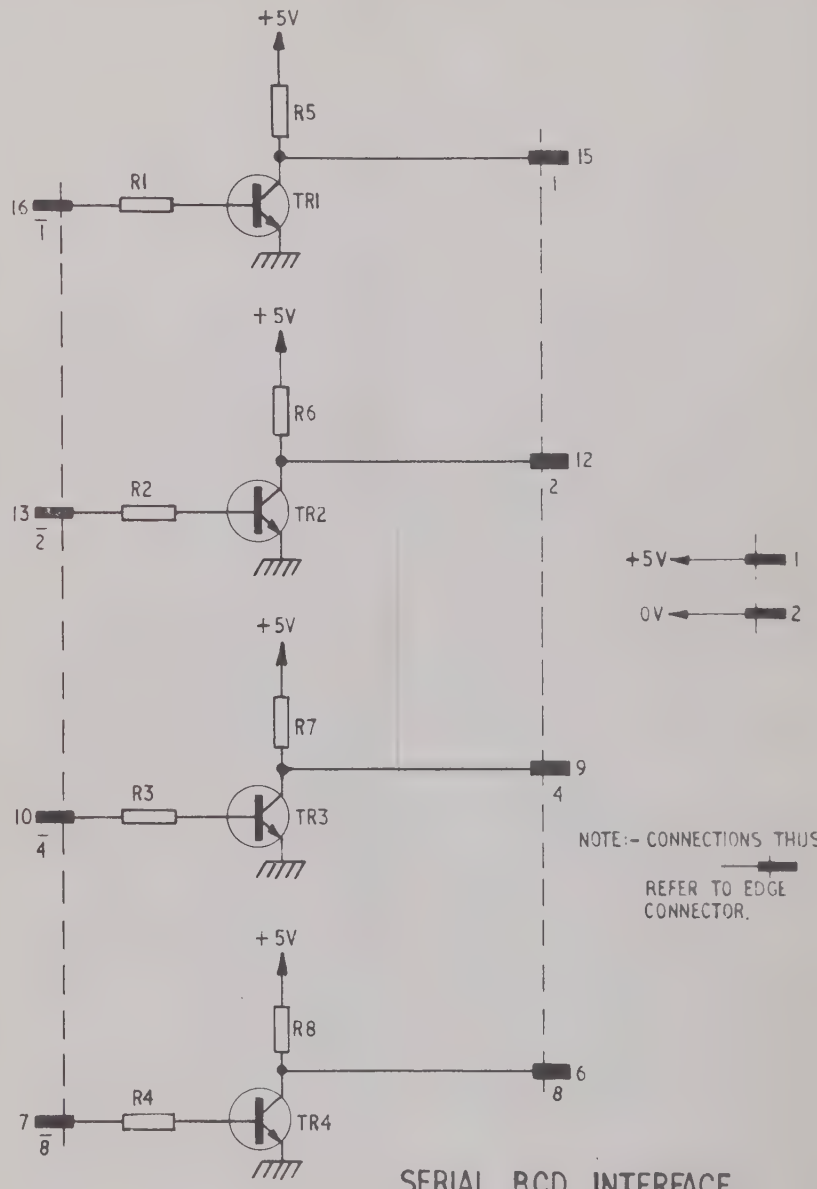
SCALE 3/4 FULL SIZE.

REF.
M2820

SERIAL B.C.D. INTERFACE

TYPE 77/910

BL
77/910



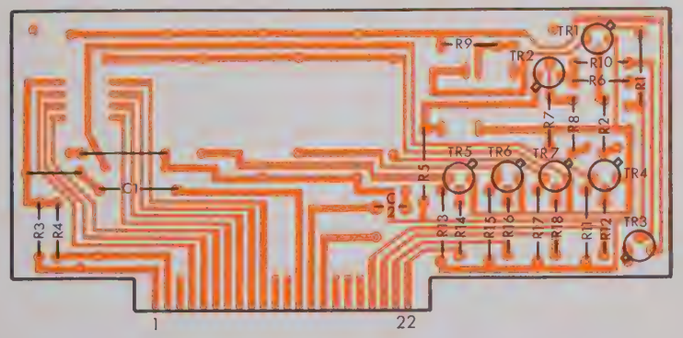
SERIAL B.C.D. INTERFACE

CIRCUIT DIAGRAM
TYPE 77/910
DRG No. E69/33

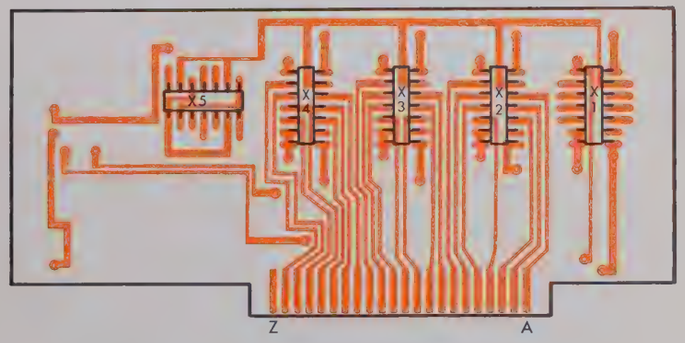
COMPONENTS LIST — CL.77/900

PARALLEL B.C.D. INTERFACE TYPE 77/900 (DRG. E69/27)

	Value or Type	Description	Venner Part No.
Capacitors			
C1	0.01µF ±10% (250V)	Polymite film	X23914/39
C2	560pF ±10%	Ceramic	Y50509/10
Integrated Circuits			
X(1-4)	SN74L164N	-	X50520/35
X5	SN74L73N	-	" /38
Resistors			
R1	1.5kΩ ± 5% ¼W HS	Carbon	X50500/53/P
R2,7	2.7kΩ ±10% 0.33W	Min. carbon film	X50517/30
R3,4	5.6kΩ " "	" " "	" /34
R5	1kΩ ± 5% ¼W HS	Carbon	X50500/49/P
R6,9	1kΩ " 0.33W	Min. carbon film	X50517/25
R8	4.7kΩ ±10% "	" " "	" /33
R10	1.5kΩ " "	" " "	" /27
R11,13,15,17	27kΩ ± 5% ¼W HS	Carbon	X50500/83/P
R12,14,16,18	8.2kΩ ±10% 0.33W	Min. carbon film	X50517/36
Transistors			
TR(1-3)	U1518/2	-	X20638/55
TR(4-7)	BC108	-	" /71



VIEWED FROM NON-COMPONENT SIDE.



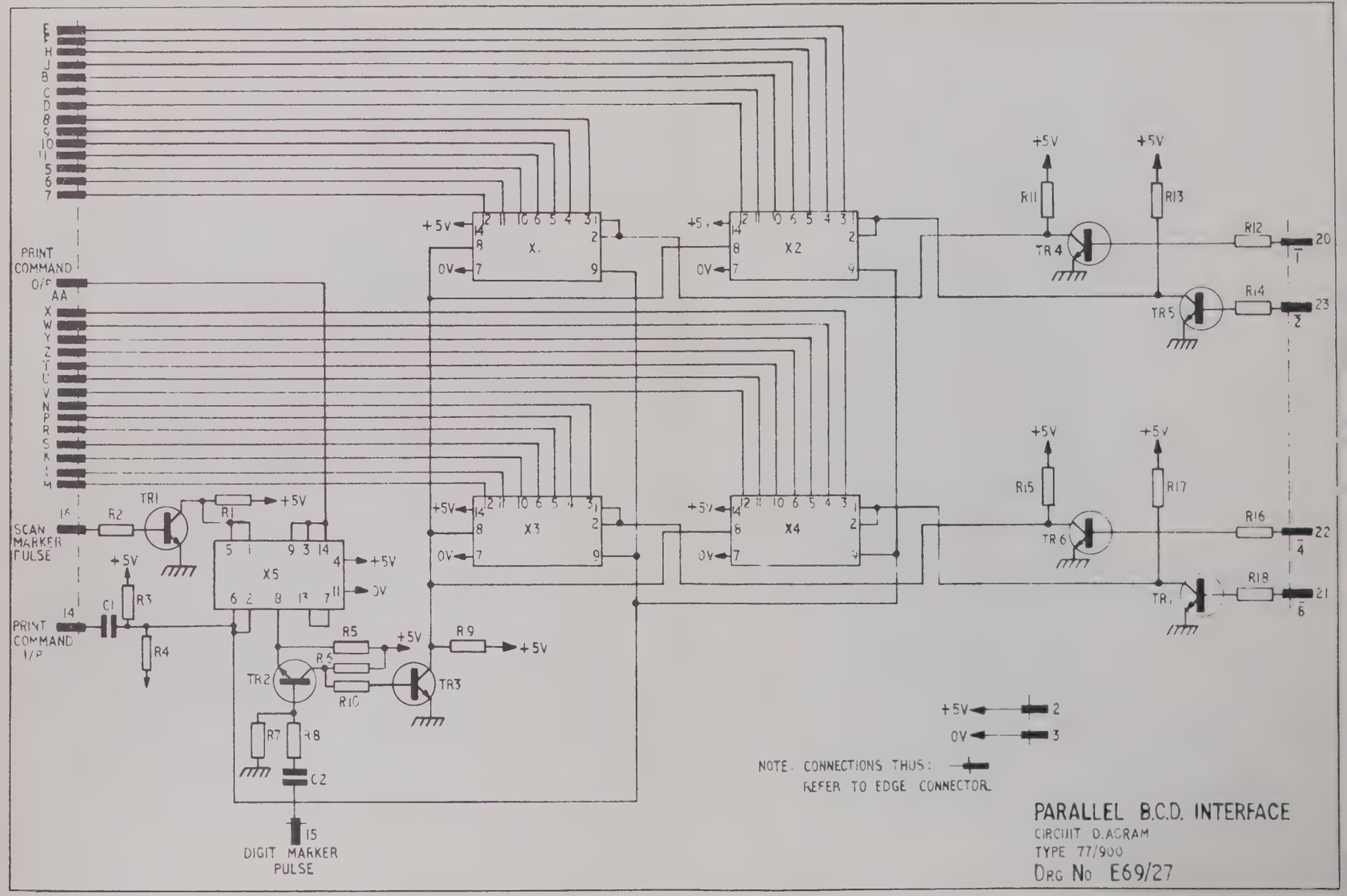
VIEWED FROM COMPONENT SIDE.

SCALE 3/4 FULL SIZE.

REF.
M2778
M2779

PARALLEL B.C.D. INTERFACE
TYPE 77/900

BL 77/900



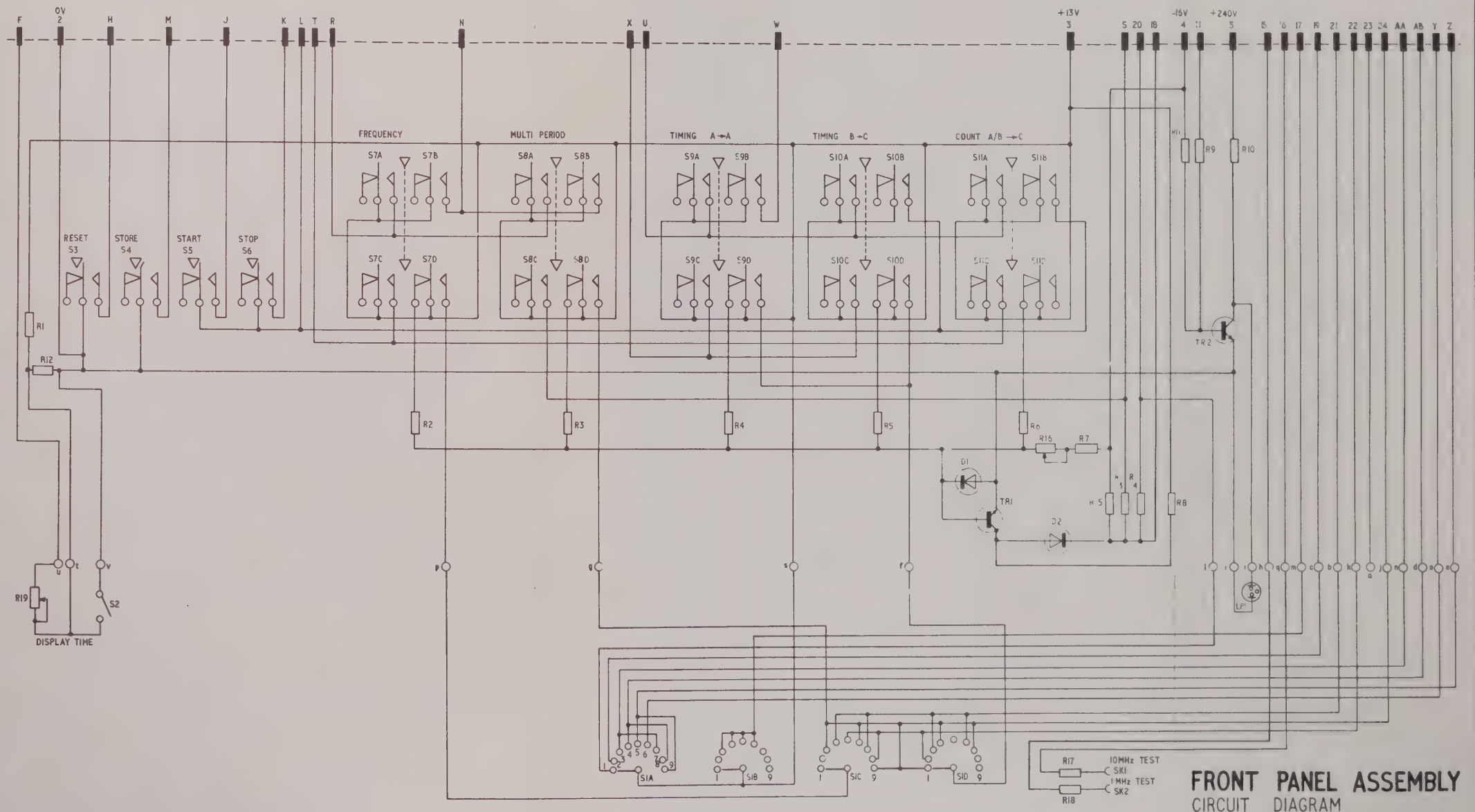
PARALLEL B.C.D. INTERFACE
CIRCUIT DIAGRAM
TYPE 77/900
DRG No E69/27

COMPONENTS LIST CL.77/010

FRONT PANEL ASSEMBLY 77/010 (DRG.E68/91)

	Value or Type	Description	Venner Part No.
Diodes			
D1,2	U2973/2	-	X20639/31/P
Indicator			
LP1	Neon	Gating Lamp	Z51400
Resistors			
R1	33kΩ ±5% ¼W HS	Carbon	X50500/85/P
R(2-6)	24kΩ " " "	"	" /82/P
R7	8.2kΩ " " "	"	" /71/P
R8	3.9kΩ " " "	"	" /63/P
R9,13,14	10kΩ " " "	"	" /73/P
R10	220kΩ " " "	"	X50501/9/P
R11	100kΩ " " "	"	" /1/P
R12	82kΩ " " "	"	X50500/95/P
R15	12kΩ " " "	"	" /75/P
R16	4.7kΩ ±20% ¼W	Carbon Lin.	X20999/63
R17,18	150Ω ±5% ¼W HS	Carbon	X50500/29
R19	500kΩ ±20% 0.2W	Carbon Lin. with ON/OFF switch	*
Sockets			
SK1,2	50S/156 (black)	Test socket	X50508/25
Switches			
S1(A-D)	2p. 9pos. rotary	Range switch	Y52052
S2	1p. ON/OFF	-	*
S(3-6)	4x1p. changeover	Push-button bank	X52051/1
S(7-11 A to D)	5x4p. changeover	" " "	" /2
Transistors			
TR1	BC108	-	X20638/71
TR2	C407	-	" /69

*R19 ganged to switch S2: common part number X20999/83.



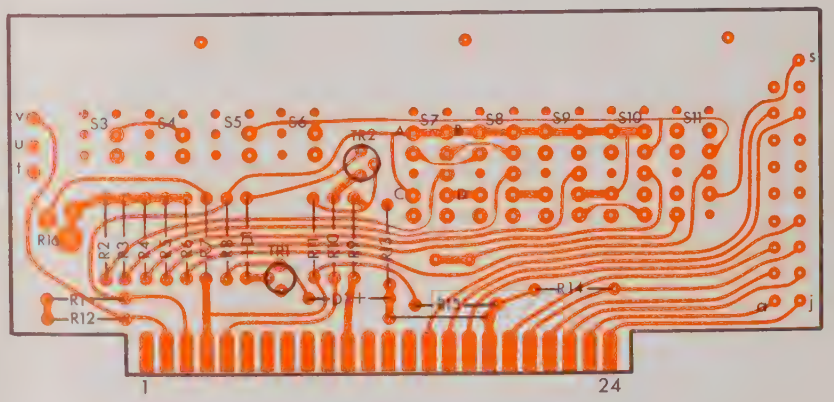
NOTE: CONNECTIONS THUS: —▮— REFER TO EDGE CONNECTOR.

FRONT PANEL ASSEMBLY

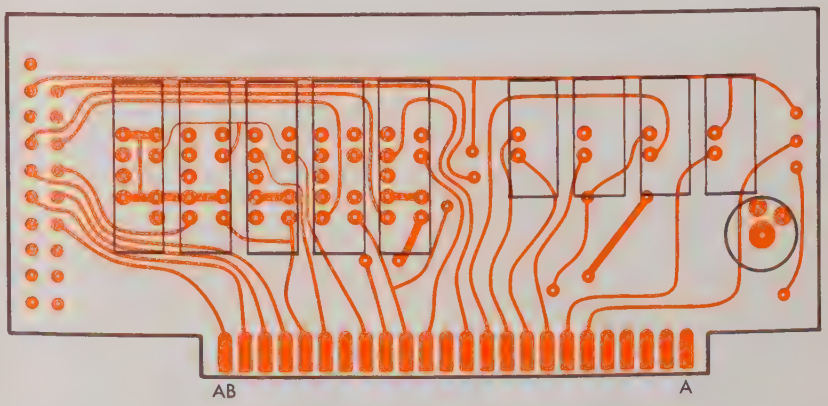
CIRCUIT DIAGRAM

TYPE 77/010

DRG. NO. E68/91



VIEWED FROM NON- COMPONENT SIDE.



VIEWED FROM COMPONENT SIDE.

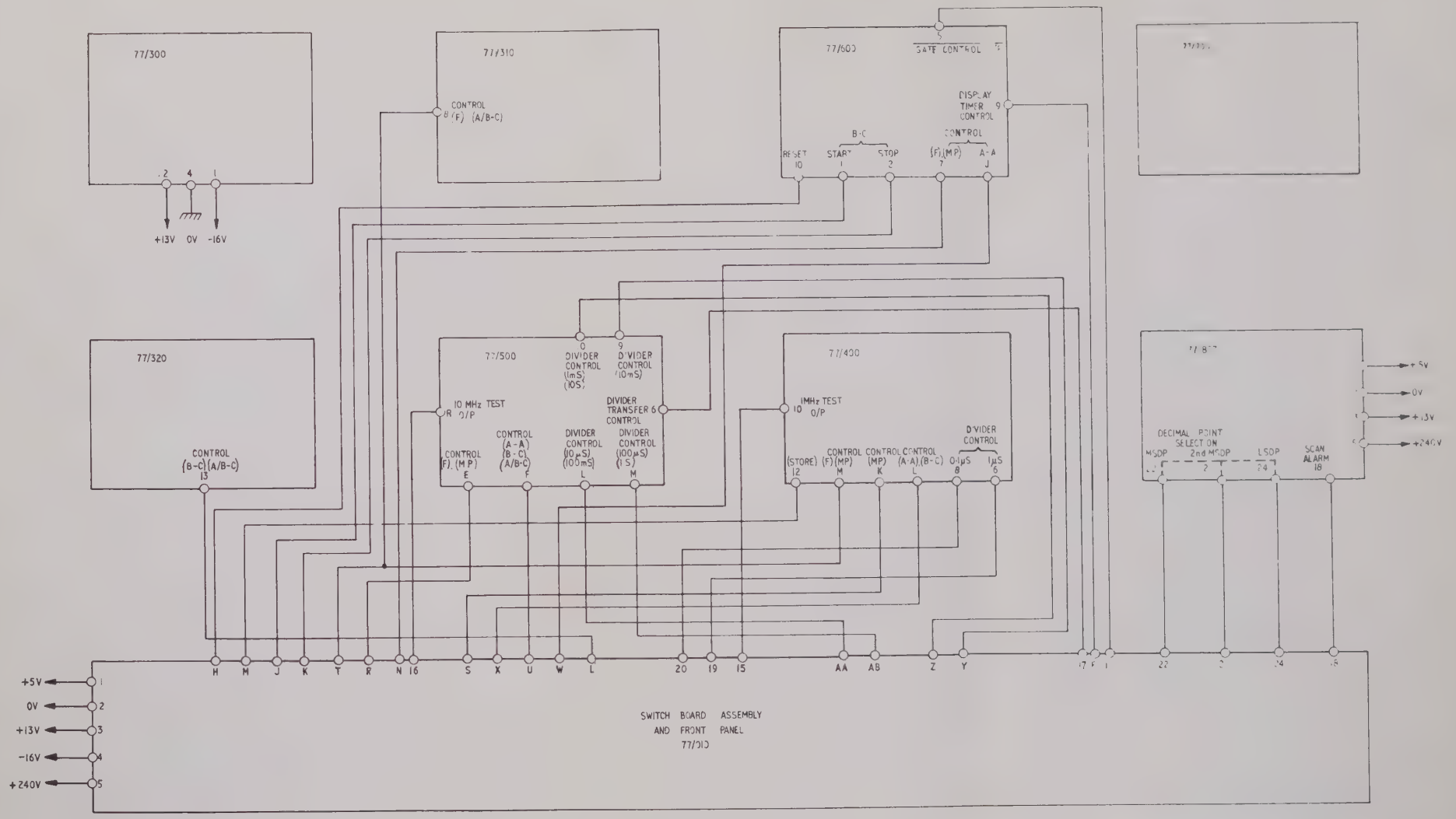
SCALE 3/4 FULL SIZE.

REF.
M2661
M2662

SWITCH BOARD

TYPE 77/010

BL 77/010



EXCEPT WHERE STATED ALL SUPPLIES AS FOLLOWS: +5V PIN 1, 0V PIN 2, +13V PIN 3, −16V PIN 4

ABBREVIATIONS USED
(F) = FREQUENCY
(MP) = MULTIPERIOD
(A-A) = TIMING (A-A)
(B-C) = TIMING (B-C)
(A/B-C) = COUNT (A/B-C)
MSDP = MOST SIGNIFICANT DECIMAL POINT
LSDP = LEAST " " "

FUNCTION CONTROL
BLOCK SCHEMATIC DIAGRAM
TYPE 7737
DRG. NO. E69/26

NOTE. CARD TYPE 77/900 FITTED ONLY FOR OPTION Z
CARD TYPE 77/910 FITTED ONLY FOR OPTION Y

77/300
TRIGGER LEVEL
'A' INPUT
PRE. AMPLIFIER
L.F. SWITCH
77/310
PULSE SHAPER PRESET
PULSE SHAPER
SLOPE SELECTION
L.F. O/P
CONTROL
MAIN GATE
GATED SIGNAL TO COUNTER
TIMING & MULTIPERIOD GATED CLOCK/DIVIDED CLOCK
REAR PANEL CONNECTOR
+13V
SLOPE SWITCH REAR PANEL
77/320
START 'B' INPUT SK1
B AMPLIFIER/ SHAPER
START PULSE
STOP 'C' INPUT SK2
C AMPLIFIER/ SHAPER
STOP PULSE
GATE CONTROL
INHIBIT
77/600
GATE CONTROL
DISPLAY TIMER
GATE CONTROL SELECTION CIRCUITS
INHIBIT
RESET
RESET PUSH BUTTON
START PUSH BUTTON
STOP PUSH BUTTON
+13V CONTROL
77/010 FRONT PANEL ASSEMBLY
GATE NEON
DISPLAY TIME POTENTIOMETER
BIAS
INF/AUTO SWITCH
T.T.L. RESET
MOS. RESET
STD SWITCH REAR PANEL
EXT
INT
77/500
EXT STD INPUT SK4
AMPLIFIER
SHAPER
10MHz XTAL OSCILLATOR
TRANSFER
RESET CONTROL
RESET 9 OSC. O/P
DUAL MOS DIVIDER
DIVIDER CONTROL
77/400
PERIOD & TIMING GATE
DECADE DIVIDER
CONTROL INTERFACE CIRCUITS
STORE TRANSFER
STORE TRANSFER TRIGGER
MOS STORE TRANSFER
TTL STORE TRANSFER
SELECTED DIVIDER O/P
MOS DIVIDER I/P
MOS DIVIDER O/P
STORE PUSH BUTTON
10 MHz TEST SKT
STD FREQ'S O/P SKT SK3
1 MHz TEST SKT
7 DIGIT COUNTER 77/700
7 DIGIT DISPLAY 77/807 & 77/817
SERIAL BCD INTERFACE 77/910
DATA OUTPUT SOCKET PIN No
0V
PARALLEL BCD INTERFACE 77/900
O/P II BCD
DATA O/P SOCKET PIN No
O/P PRINT COMMAND
MSD
LSD

UNIT DESIGNATION

No.	COLOUR	TITLE
77/300	—	PREAMPLIFIER
77/310	RED	PULSE SHAPER
77/700	BLUE	COUNTER
77/600	BEIGE	GATE CONTROL & RESET
77/500	GREEN	OSCILLATOR & DIVIDER
77/320	PINK	START/STOP SHAPERS
77/807	—	DISPLAY
77/817	—	DISPLAY CONTROL
77/010	—	FRONT PANEL ASSEMBLY
77/020	—	REAR PANEL ASSEMBLY
77/220	—	POWER SUPPLY
77/900		PARALLEL BCD INTERFACE
77/910		SERIAL " "

MAINS SUPPLY
LIVE
NEUTRAL
EARTH
S1
FS1
L1
L2
C1a
C1b
C1c
REAR PANEL CONNECTOR
POWER SUPPLY 77/220
TO SELECTED TAPPINGS OF TRANSFORMER
PIN 5 +5V
PIN 4 0V
PIN 6 +13V
PIN 7 -16V
PIN 1 +240V
FOR CONNECTIONS TO THE VARIOUS MODULES REFER TO DRG E69/26

DIGITAL COUNTER
SIGNAL PATH DIAGRAM
TYPE 7737
DRG. NO E69/25

APPENDIX

COUNTER TYPE 77/710 FITTED IN MODEL 7737A

Circuit Description:

Terminations at the edge-connector of this plug-in card are the same as those of Counter card type 77/700 described in Section 5.10.

The circuit of Counter type 77/710 is shown on diagram E69/23. Two flip-flops X3 and X5 (Schottky-clamped) and quad-two-input NAND-gate X4 are connected to form a high frequency (80MHz) decade counter for input pulses received at termination 5.

Thereafter the circuit is almost identical in design to that of Counter type 77/700 shown on diagram E68/98. Circuit stages X7, TR1, X1, X2 and X9 of Counter type 77/700 correspond respectively to circuit stages X1, TR1, X3, X4 and X5 of diagram E68/98; however, because an h.f. input decade is used in Counter type 77/710 the second half of double decade integrated circuit X9 (drg. E69/23) is unused.

In the circuit of Counter type 77/710, integrated circuit X6 serves as store for count information held by the h.f. decade; its action is similar to that of store X8, which corresponds to integrated circuit X2 of diagram E68/98.

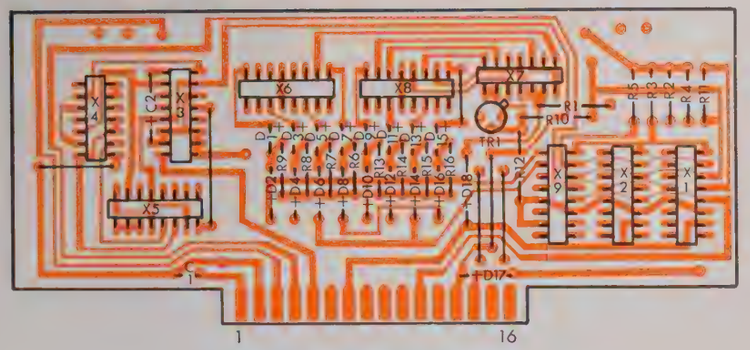
Circuit, Components List and Layout Diagram:

Diagram E69/23 showing the circuit of Counter type 77/710, and corresponding components list CL77/710 and layout diagram BL.77/710 are provided overleaf.

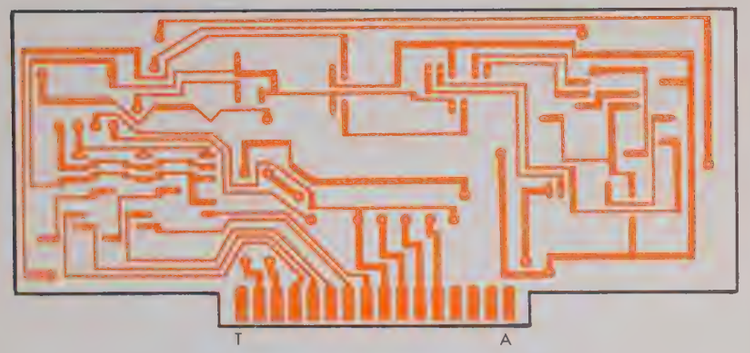
COMPONENTS LIST _____ CL.77/710

COUNTER 80MHz TYPE 77/710 (DRG. E69/23)

	Value or Type	Description	Venner Part No.
Capacitors			
C1	0.047uF +50% -25%	Polystyrene & Ceramic	X20641/55
C2	2.2µF (20V)	Tantalum	X22776/22
Diodes			
D(1-17)	U2973/2	-	X20639/31
D18	AAZ17	-	" /63/P
Integrated Circuits			
X1,2,9	C16	-	X50520/24
X3,5	SN74S112N	-	" /31
X4	SN74S00N	-	" /25
X6,8	SN7475N	-	" /23
X7	SN7490N	-	" /5
Resistors			
R1	3.9kΩ ±5% ¼W HS	Carbon	X50500/63/P
R(2-5)	2.7kΩ " ⅛W	Carbon film	X50517/30
R(6-9),(13-16)	12kΩ " "	" "	" /38
R10	2.4kΩ " ¼W HS	Carbon	X50500/58/P
R11	1.5kΩ " ⅛W	Carbon film	X50517/27
R12	430Ω " ¼W HS	Carbon	X50500/40/P
Transistor			
TR1	U1518/2	-	X20638/55



VIEWED FROM NON-COMPONENT SIDE.



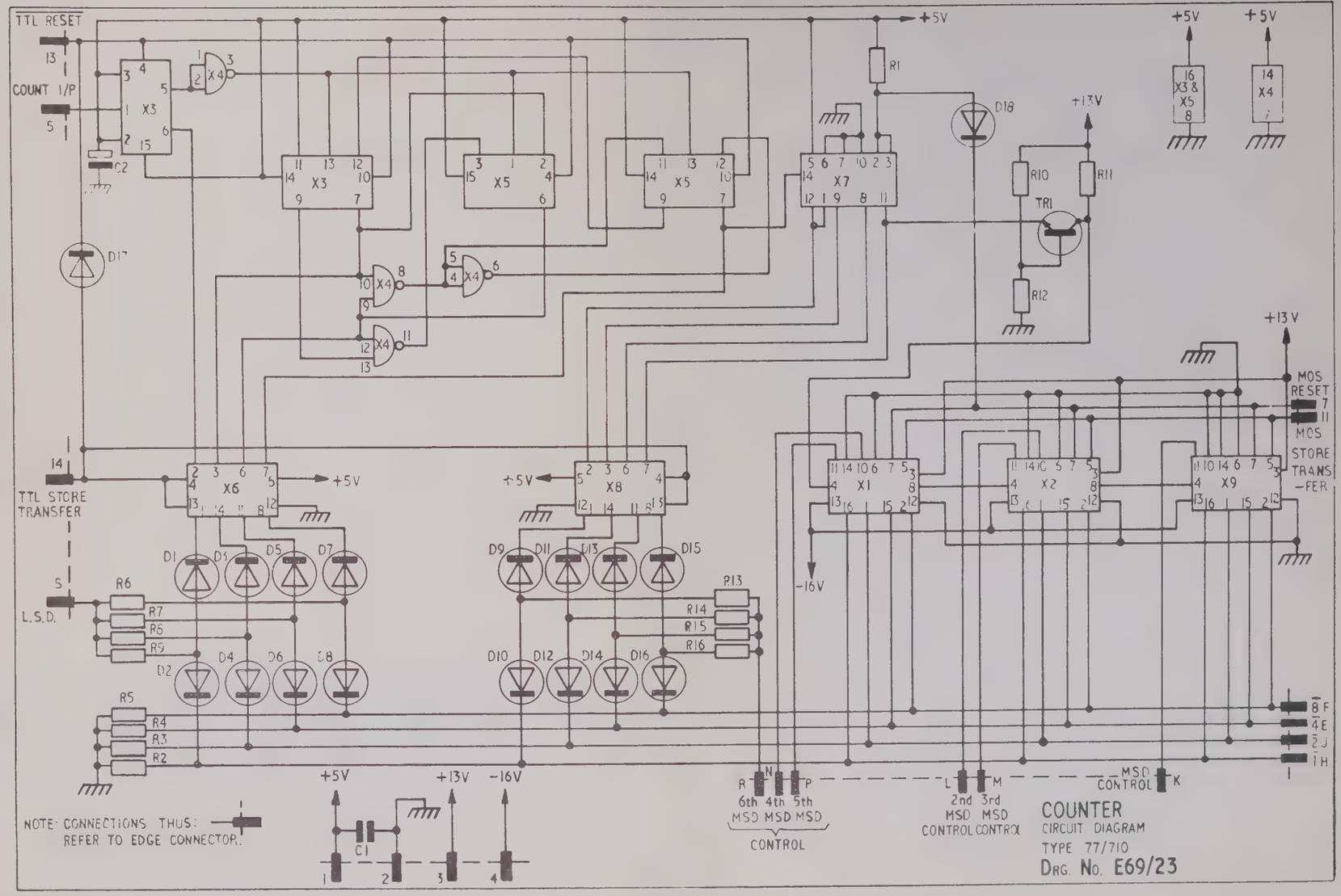
VIEWED FROM COMPONENT SIDE.

SCALE 3/4 FULL SIZE.

REF
M2763
M2764

COUNTER
TYPE 77/710

BL
77/710



CORRIGENDA
Digital Counter Model 7737
Instruction Manual

CHANGE IN TYPE OF 'DISPLAY TIMER' & 'TRIGGER LEVEL' CONTROLS

The DISPLAY TIMER and TRIGGER LEVEL potentiometers carry a ganged switch operable at one end of the track. The manual states this end as being the CLOCKWISE end.

During 1973 potentiometers with the switch operable at the ANTI-CLOCKWISE end were introduced into the manufacture of the counters. Instruments fitted with this later type of control have the legends 'LF' and 'INF' at the anti-clockwise ends of the Trigger Level and Display Timer panel-inscriptions, respectively, and for these units the following amendments are applicable to the manual.

Page 9, Section 3.5.2 (under 'Trigger Level LF Position'), and
Page 10, Section 3.5.4:
For 'fully clockwise' read 'fully anti-clockwise'.

Components Lists CL77/300 and CL77/010:
In footnote: for 'X20999/83' read 'X20999/97'.

SPECIFICATION Page 2 : In Section '2.3.2 Multi-period' the Accuracy should appear thus:

Accuracy: ± 0.1μs ± crystal stability ± input circuit jitter.

Input circuit jitter — Range 1 : 0.3%
,, 10 : 0.03%
,, 10^2: 0.003%
Similarly for subsequent ranges the error is progressively reduced by a factor of 10.

1. DATA OUTPUT FACILITY: Page 21 Section 3.11 2nd para:

For '1-2-4-2 code' read '1-2-4-8 code'

2. Oscillator & Divider type 77/511:

Drg. No.E69/22 & BL77/511: Resistors R16 & R17 are not fitted on card type 77/511.

CL77/510 & 511: Against R16 read:
3.9kΩ ±5% ¼W HS Carbon X50500/63/P

Note R16 & R17 are not fitted on card type 77/511.

To line commencing R4 delete '4'
Add to list:
R4 2.2kΩ ±5% ⅛W Carbon X50517/29

3. Stop & Start Shapers type 77/320:

CL77/320 : Delete asterisk against transistors TR1 & TR8 and delete associated footnote.

Drg. E69/01 : Against Pin 12 for '-ve' read '+ve'
" " 10 " '+ve' " '-ve'

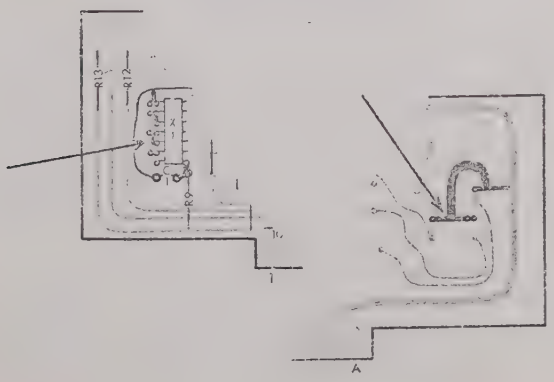
4. Counter type 77/700:

Drg. E68/98 : Pins 3,4,10 & 11 of integrated circuit X1 should appear connected to chassis-earth and not to the junction C1/R9 as shown.

BL77/700 : (i) Delete component positions R20 and TR3.

(ii) The layout of copper tracks in the region of X1 should be amended thus:

NOTE Track changes are shown arrowed.



5. Switch Board type 77/010:

Drg. E68/91 & BL77/010: A capacitor (C1) should appear connected between points 'r' and 'h'(on Drg.E68/91 adjacent to LP1; on BL77/010 near top right-hand corner of upper figure).

CL77/010 : Add C1 100 to 220pF ±10% cermaic; preferred value 150pF Venner Part No. X20641/44.

6. Power Supply type 77/220:

BL77/220 : For termination pad numbers 1,2,3,4,5,6 read 1,5,6,4,2,3

CL77/220 : Against C1 for '8µF(350V)' read '10µF(400V)'
For 'C(8-10)' read 'C8,10'
Add C9 6.8µF 35V Y50518/6
For C2 read 1000µF (63V) Electrolytic X20643/96
For C3 read 2200µF (16V) Alumin. foil " /68
For R2,3 read 470Ω ±20% ¼W Carbon lin.X20999/98

7. Pre-Amp type 77/300:

Drg.E68/95, BL77/300, CL77/300 } Delete C7

CL77/300: Under TRANSISTORS
For BFY90 X20638/95
read 2N5179 X50528/10

8. Pulse Shaper type 77/310:

Drg.E68/94 : Add C11 between chassis-earth (negative) and TR1 emitter.

BL77/310 : Pads for TR1 slightly re-positioned and C11 added between TR1 and C2.

CL77/310 : Add C11 33µF . 10V Y50518/2
Delete R13, and for 'R11' read 'R11, 13'
Against X1,2 for 'SN7300N' read 'SN74S00N'
Against R4 for '4.3kΩ' read '3.3kΩ' and for '/64/P' read '/61/P'.
Under TRANSISTORS:
For BFY90 X20638/95
read 2N5179 X50528/10.

9. Oscillator and Divider type 77/511:

Drg.E69/22 : Delete R15 and connect X5 '+V' termination to +5V line

BL77/511 : Copper track altered for above connection.

CL77/511 : Delete R15 of card type 77/511

10. Gate Control & Reset type 77/600:

Circuit description Section 5.9..
Page 43 line 15: for 'X2(13)' read 'X3(13)'.
Page 44 line 12: for '1' read '0'

CL77/600 : Against TR6, for type V4054' read 'V405A'

Drg.E68/99 : Designations 'C11' & 'C12' should be interchanged.

11. Display Control type 77/817:

CL77/817 : Against Diodes D(1-7) read 'BYX10 X20639/70'

12. Parallel BCD Interface type 77/900:

Drg.E69/27 : Delete R5
Add diode D1 between TR3-base (cathode) and R10.
Add C3 in parallel with R10

BL77/900 : Copper tracks altered and references added for above modification
Top view: For edge connection '1' read '2'
" " " '22' " '23'
Lower view: For edge connection 'Z' read 'AA'
" " " 'A' " 'B'

CL77/900 : Delete R5, R8 and R10.
For 'C2' read 'C2, 3'
Add Diode D1 U2973/2 X20639/31.
For 'R3,4' read 'R3,4,10'
For R6 read 4.7kΩ ±10% 0.33W X50517/33
To 'R12,14,16,18' add R8.
Against R9 read: 22kΩ ±5% Carbon film X50517/41

13. Function Control Diagram E69/26:

Above termination 'M' in block 77/400
for '(F) (MP)' read '(F) (A/B-C)'
At block 77/300 show capacitor C1 connected between termination 4 and additional termination 6, and C2 connected between termination 4 and additional termination 7.
C1 & 2: 0.047µF Disc X20641/55.

14. Components Lists CL77/... 320,400,500,510 & 511,600,700 & 900:
For transistor type 'U1518/2' read 'U15718/2'.

15. Components List CL77/500:
Under RESISTORS:
In line commencing R3 delete '28'.
Add to list:
R28 2.2kΩ ±5% $\frac{1}{8}$W Carbon film X50517/29

Under CAPACITORS:
Against C8 read: 4.5-20 pF air-spaced trimmer X21135/17.

16. Components List CL77/300:
(Venner ref. Mod.1) Under DIODES
Delete line commencing 'D1,2..'
In line commencing D4 for 'D4' read 'D1,2,4'.

17. Components List CL77/310:
Under DIODES
Delete line commencing 'D3'
In line commencing D2 for 'D2' read 'D2,3'.

18. Board Layout BL77/510 & 511:
(Venner ref. Mod.1) Copper layout in region C8/TR3 has been slightly rearranged.

MP MASTER
MA24445

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